Overview of VLSI

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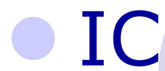
- VLSI
  - **V**ery-**L**arge-**S**cale **I**ntegration
- Today's complex VLSI chips
  - The number of transistors has exceeded 120 million
  - Die area is typically about $1 cm^2$
- Moore's low (Gordon Moore, one of the cofounders of the Intel Corporation)
  - The number of transistors on a chip would double about every 18 months
- Design team and design hierarchy are needed to realize a complex chip

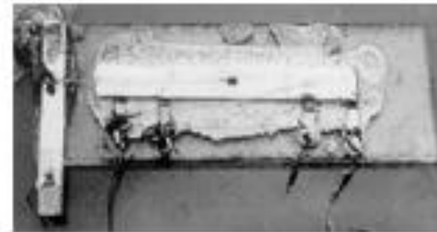


- IC
  - Integrated circuit
- ICs have three key advantages over digital circuits built from discrete components
  - Small size
    - ICs are much smaller, both transistors and wires are shrunk to micrometer sizes, compared to the centimeter scales of discrete components
  - High speed
    - Communication within a chip is faster than communication between chips on a PCB
  - Low power consumption
    - Logic operations within a chip take much less power

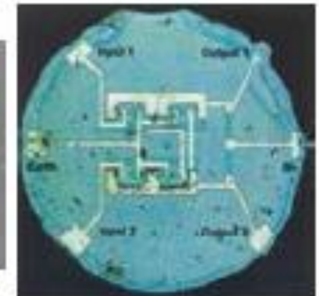
Milestones for IC Industry

- 1947: Bardeen, Brattain & Shockly invented the transistor, foundation of the IC industry.
- 1952: SONY introduced the first transistor-based radio.
- 1958: Kilby invented integrated circuits (ICs).
- 1965: Moore’s law.
- 1968: Noyce and Moore founded Intel.
- 1970: Intel introduced 1 K DRAM.

First transistor



First IC by Kilby



First IC by Noyce

Milestones for IC Industry

- **1971:** Intel announced 4-bit 4004 microprocessors (2250 transistors).
- **1976/81:** Apple II/IBM PC.
- **1984:** Xilinx invented FPGA's.
- **1985:** Intel began focusing on microprocessor products.
- **1987:** TSMC was founded (fabless IC design).
- **1991:** ARM introduced its first embeddable RISC IP core (chipless IC design).

Intel founders

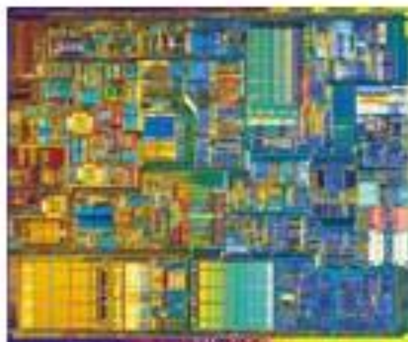
4004

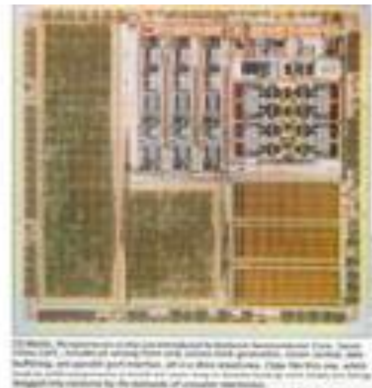
IBM PC

Milestones for IC Industry (Cont’d)

- 1996: Samsung introduced IG DRAM.
- 1998: IBM announces1GHz experimental microprocessor.
- 1999/earlier: System-on-Chip (SOC) applications.
- 2002/earlier: System-in-Package (SIP) technology.
- An Intel P4 processor contains 42 million transistors (1 billion by 2005)
- Today, we produce > 30 million transistors per person (1billion/person by 2008).

4GB DRAM (2001)


Pentium 4


Scanner-on-chip

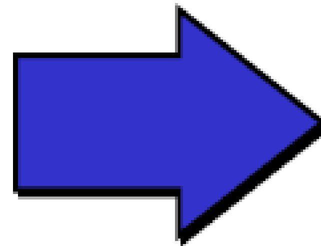
Blue tooth technology

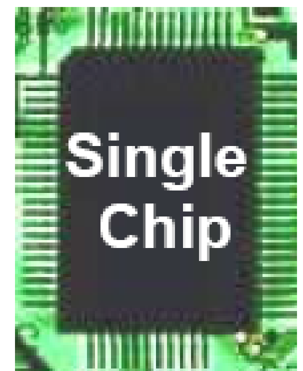
A Representative 2G/2.5G Cell Phone

Today's Cell Phone

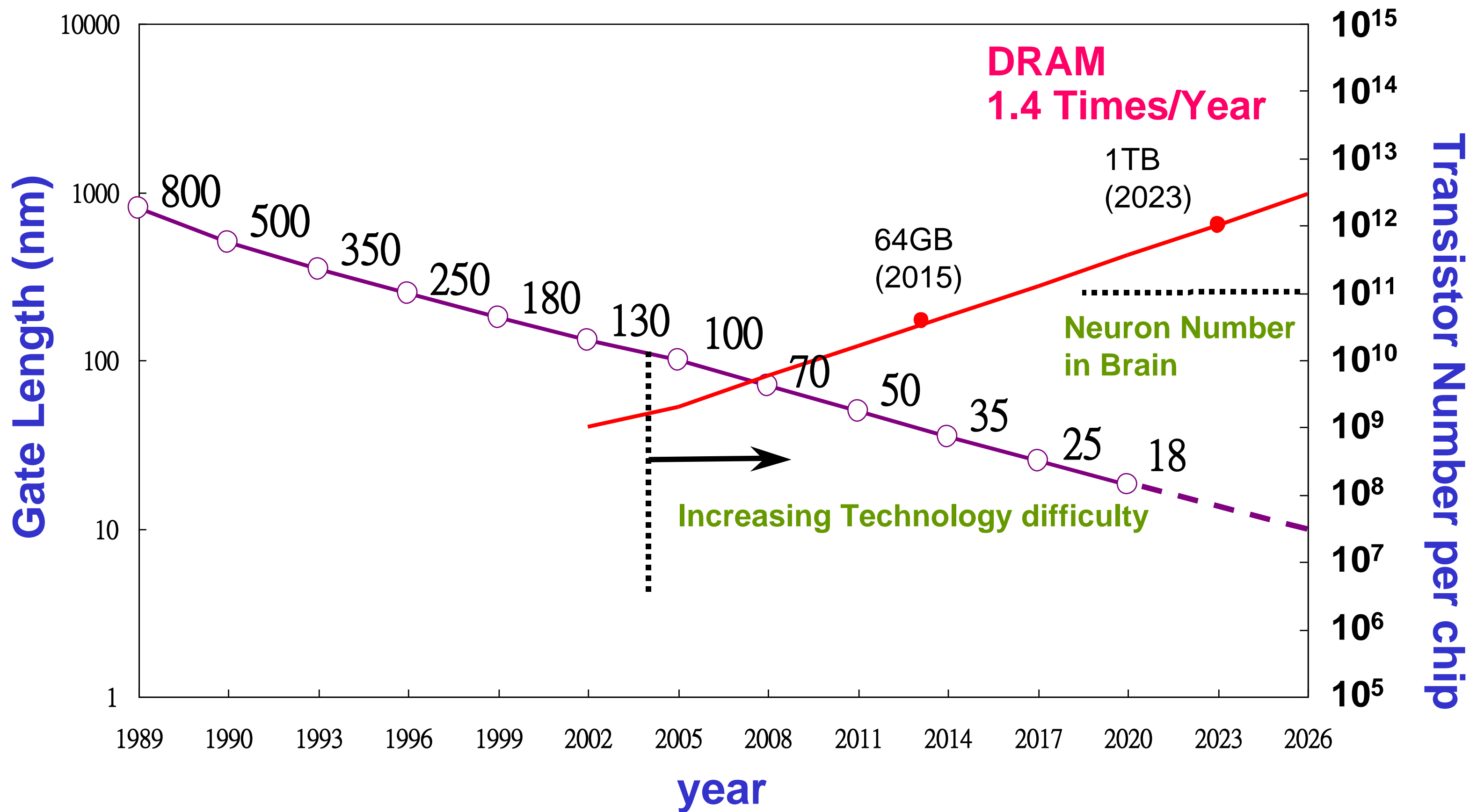
- DSP
- RAM
- FLASH
- Radio
- Analog
- Power Management
- Passives
- Discretes

SOC Integration

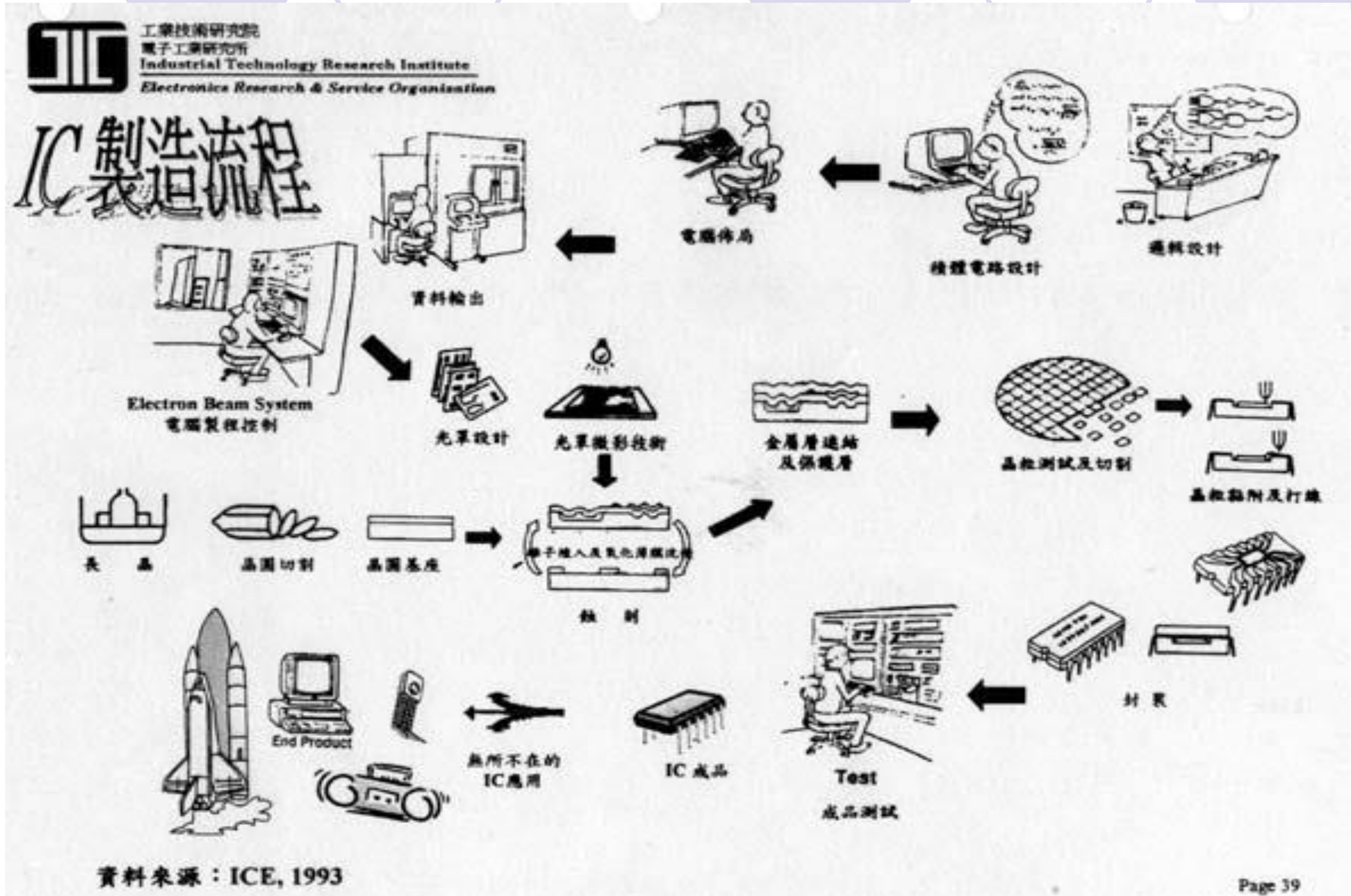




Technology Evolution

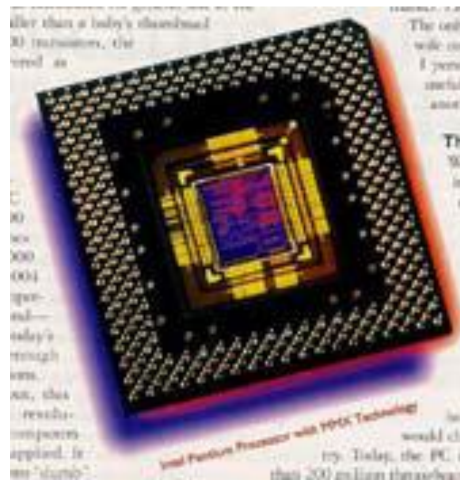


IC Design & Manufacturing Process

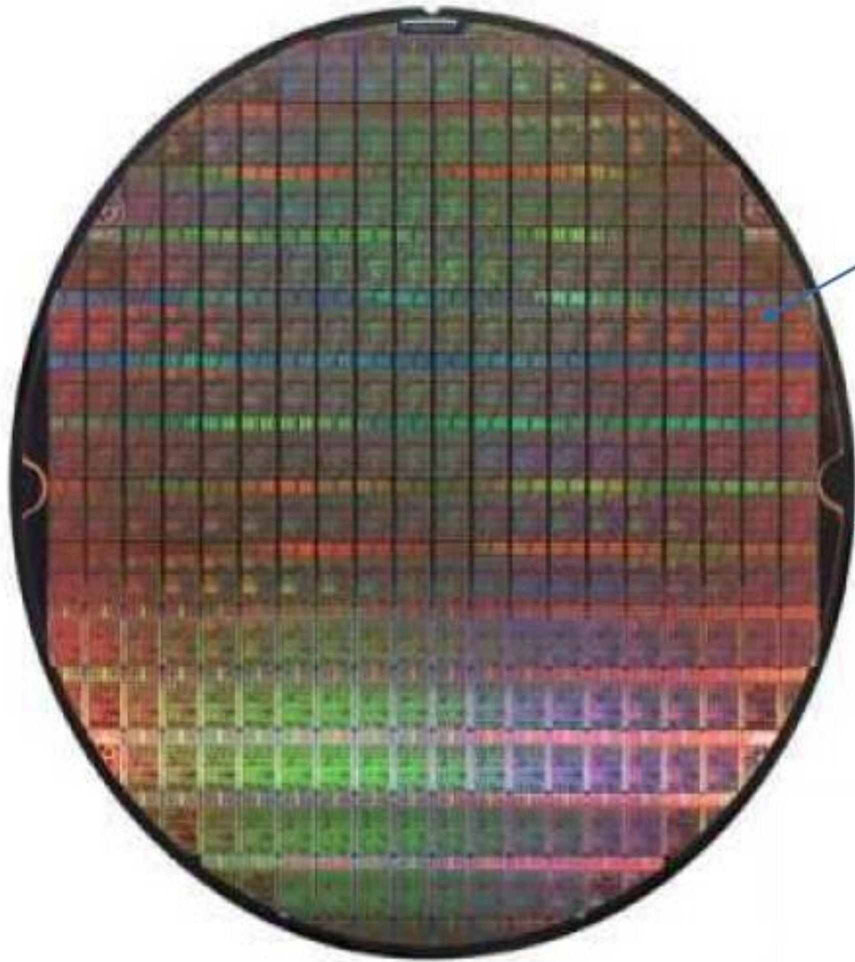


From Wafer to Chip

Figure 9-34 Attachment of leads from the Al pads on the periphery of the chip to posts on the package. (Photograph courtesy of Motorola, Inc.)



Wafer

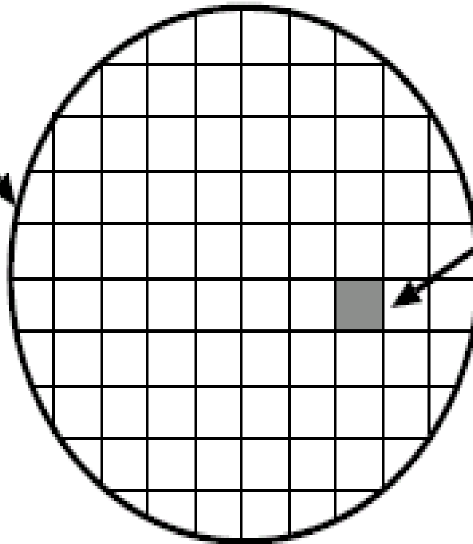


Single die

Wafer

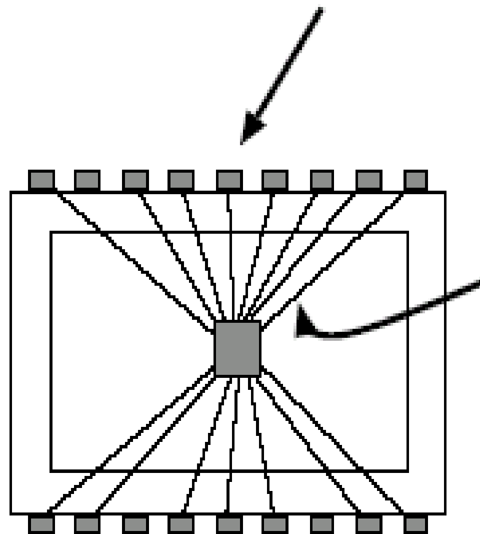
Going up to 12″ (30cm)

Silicon wafer



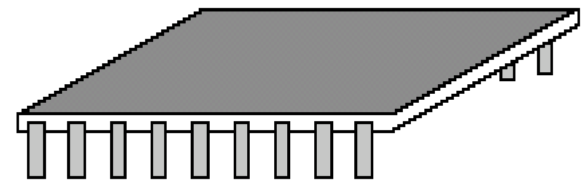
chip

pin

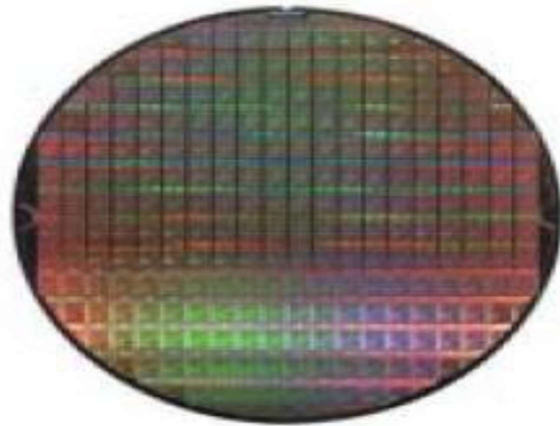


chip-to-pin wire

Enclosed chip
(IC package)



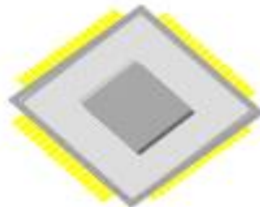
Manufacturing Flow



Sawing & Packaging

Chips

Testing

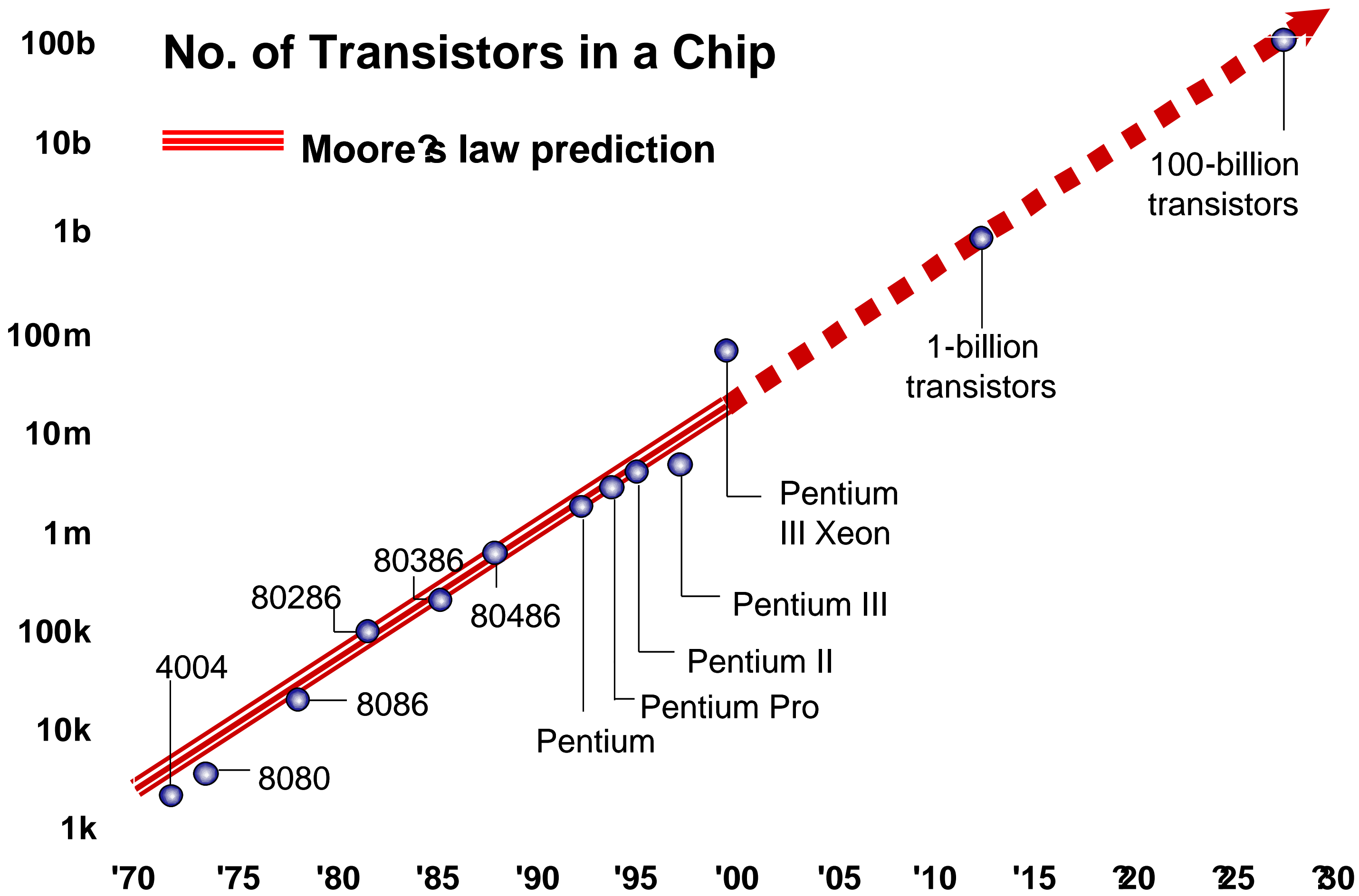


Bad chips

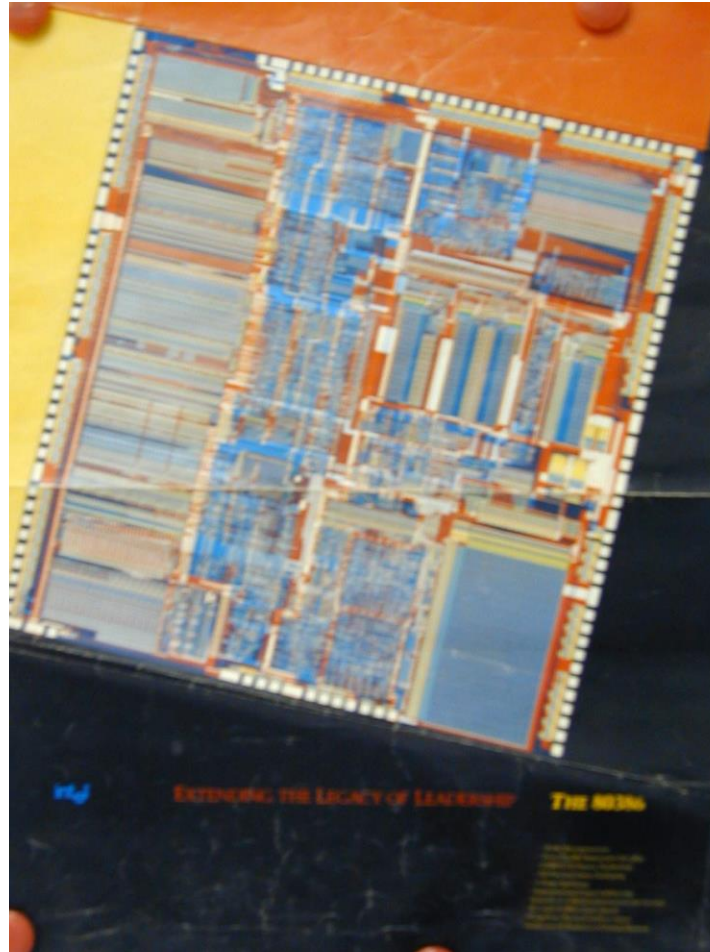
Good chips

Customers

CPU Evolution



32-bit CPU 80386



Traditional VLSI Design Cycle

System Specification

functional simulation

specification

Function/architecture Design

logic simulation

behaviorial representation

Logic Synthesis

circuit analysis

structural representation

Circuit Design

extraction & verification

structural representation

$Z = \overline{a + bc + de}$

a
b
c
d
e
Z

V_{DD}
b
c
a
1
2
d
e
Z
b
3
a
d
4
c
e
V_{SS}

extraction &
verification

structural
representation

Physical Synthesis

physical
representation

c b a e d

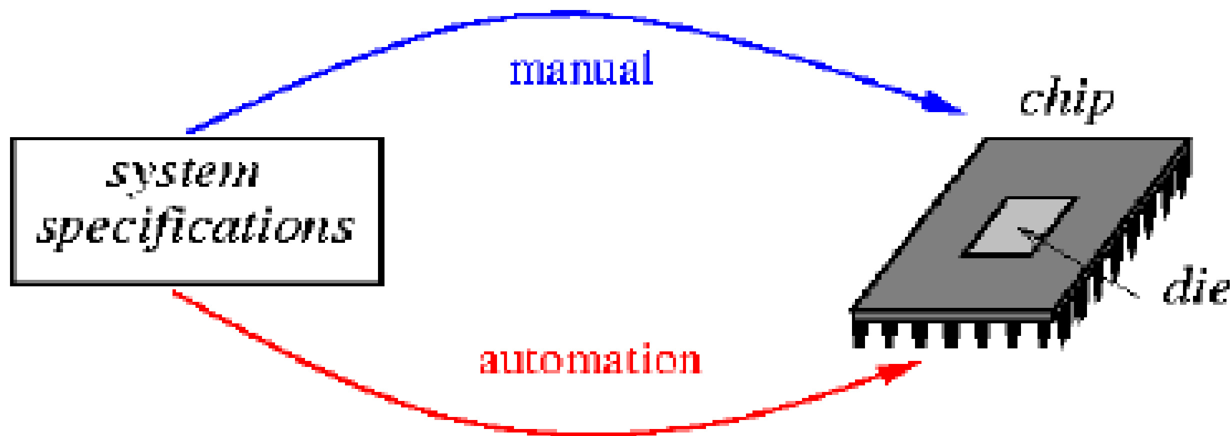
Fabrication

Packaging

IC Design Considerations

Several conflicting considerations:

1. **Design Complexity:** large number of devices/transistors
2. **Performance:** optimization requirements for high performance
3. **Time-to-market:** about a 15% gain for early birds
4. **Cost:** die **area**, packaging, testing, etc.
5. Others: power, signal integrity (noise, etc), testability, reliability, manufacturability, etc.



Nanometer Design Challenges

- In 2005, feature size ≈ 0.1 μ*m*, μP frequency ≈ 3.5 GHz, die size ≈ 520 mm2, μP transistor count per chip ≈ 200M, wiring level ≈ 8 layers, supply voltage ≈ 1 V, power consumption ≈ 160 W.

Feature size **sub-wavelength lithography (impacts of process variation)? noise? wire coupling? reliability?**

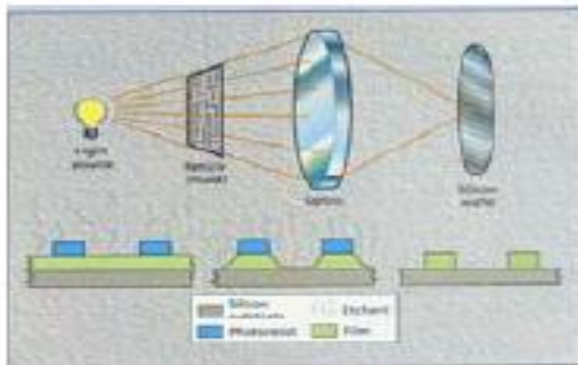
Frequency , dimension **interconnect delay? Electromagnetic field effects? timing closure?**

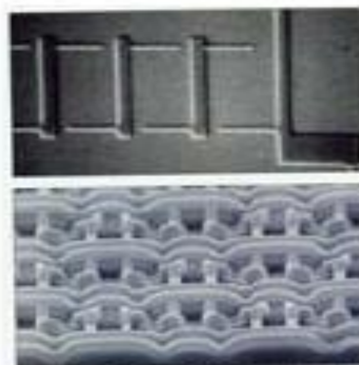
Chip complexity **large-scale system design methodology?**

Supply voltage **signal integrity (noise, IR drop, etc)?**

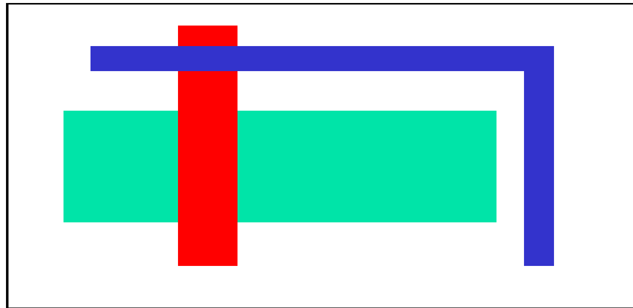
Wiring level **manufacturability? 3D layout?**

Power consumption **power & thermal issues?**

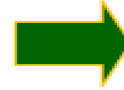


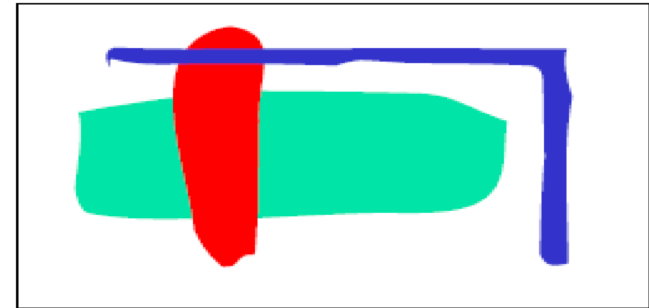


Sub-wavelength Lithography Causes Problems!!

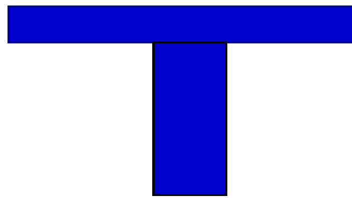


Mask patterns

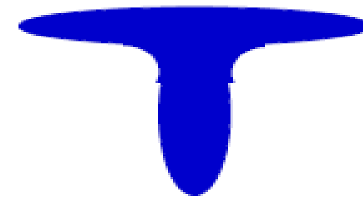




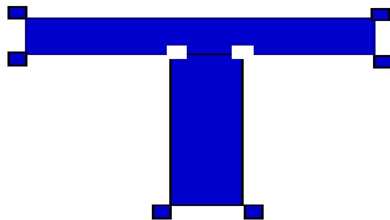
Printed layout



Drawn layout



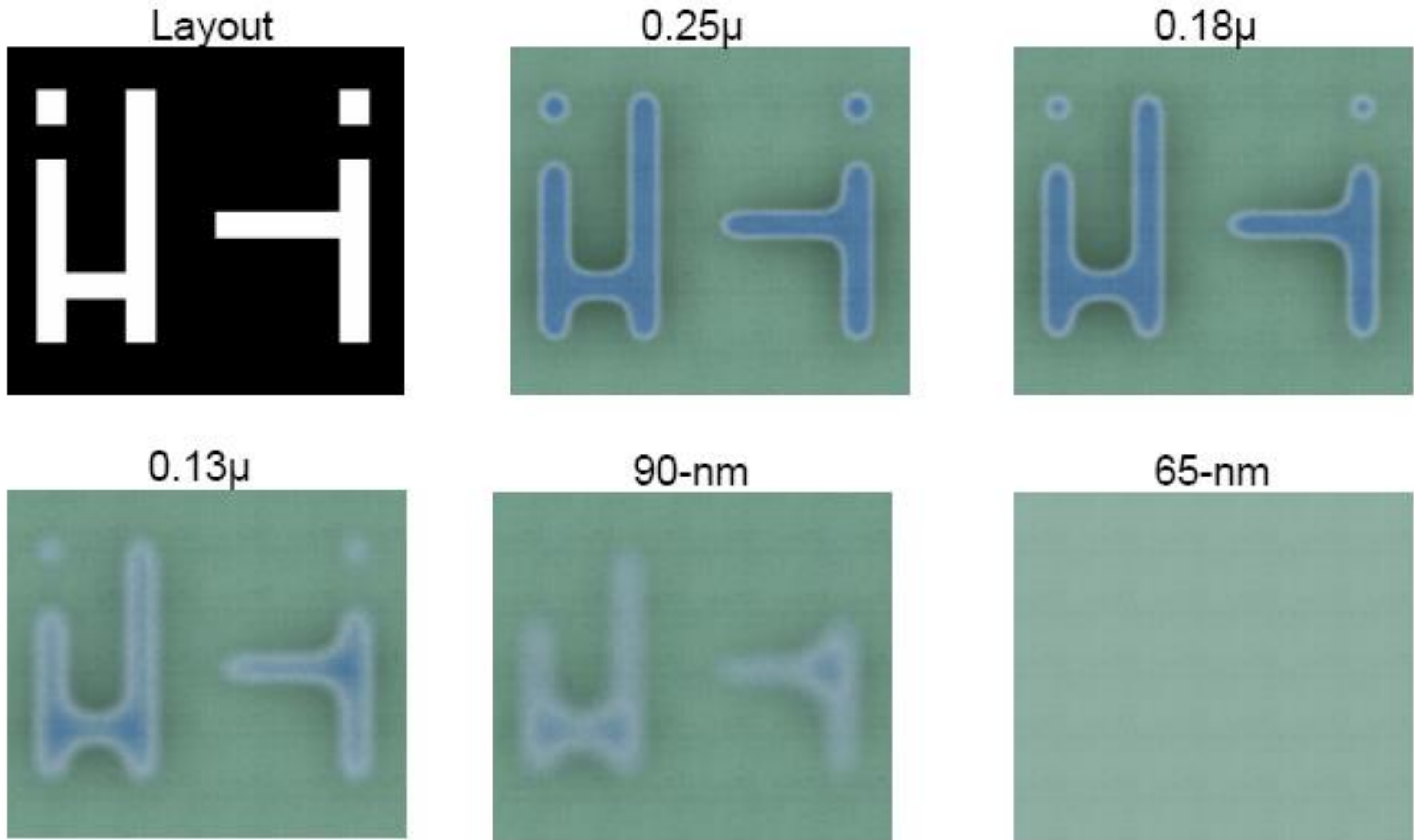
Printed wafer



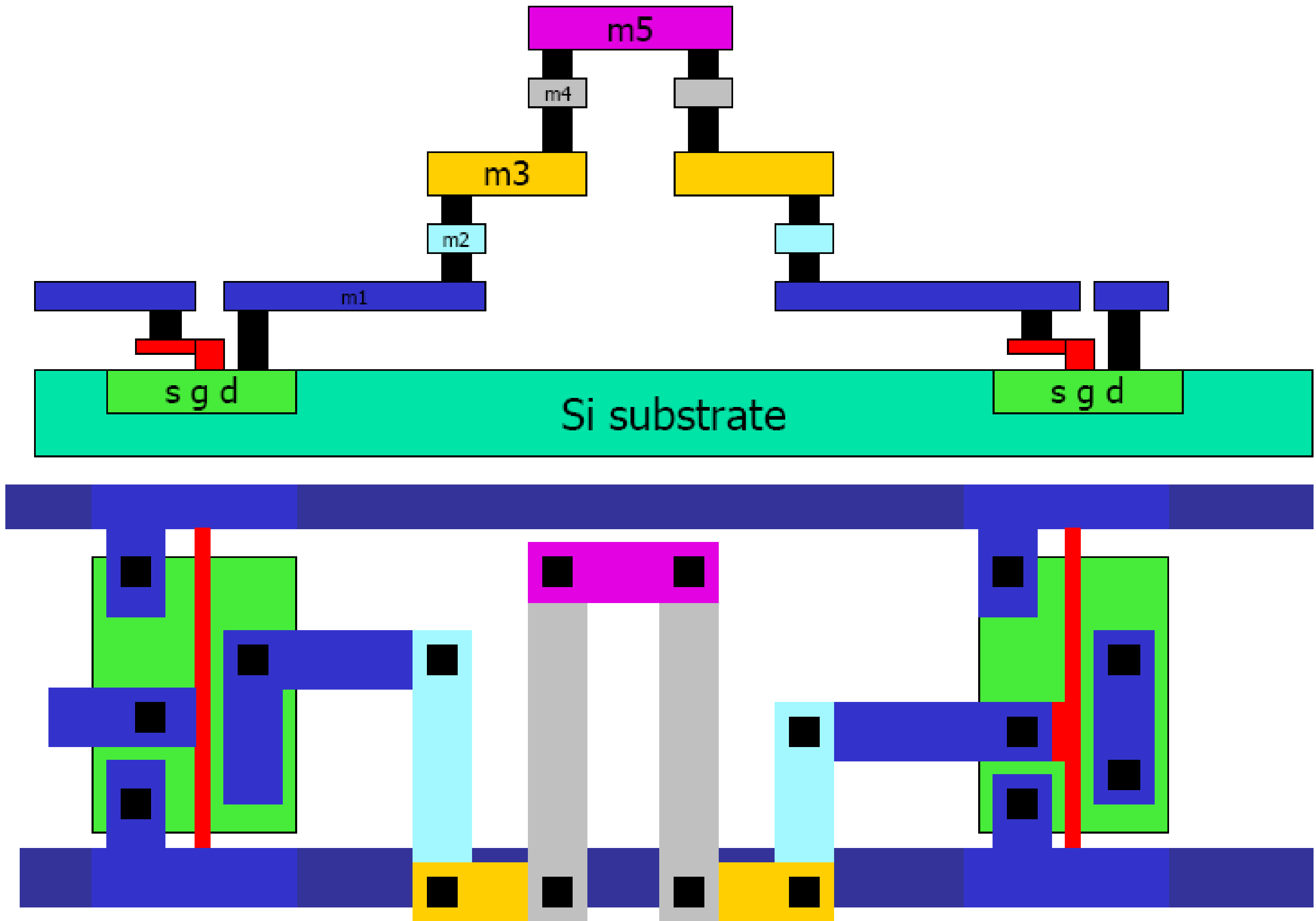
Proximity corrected layout

Printed wafer

Sub-wavelength Lithography Causes Problems!!

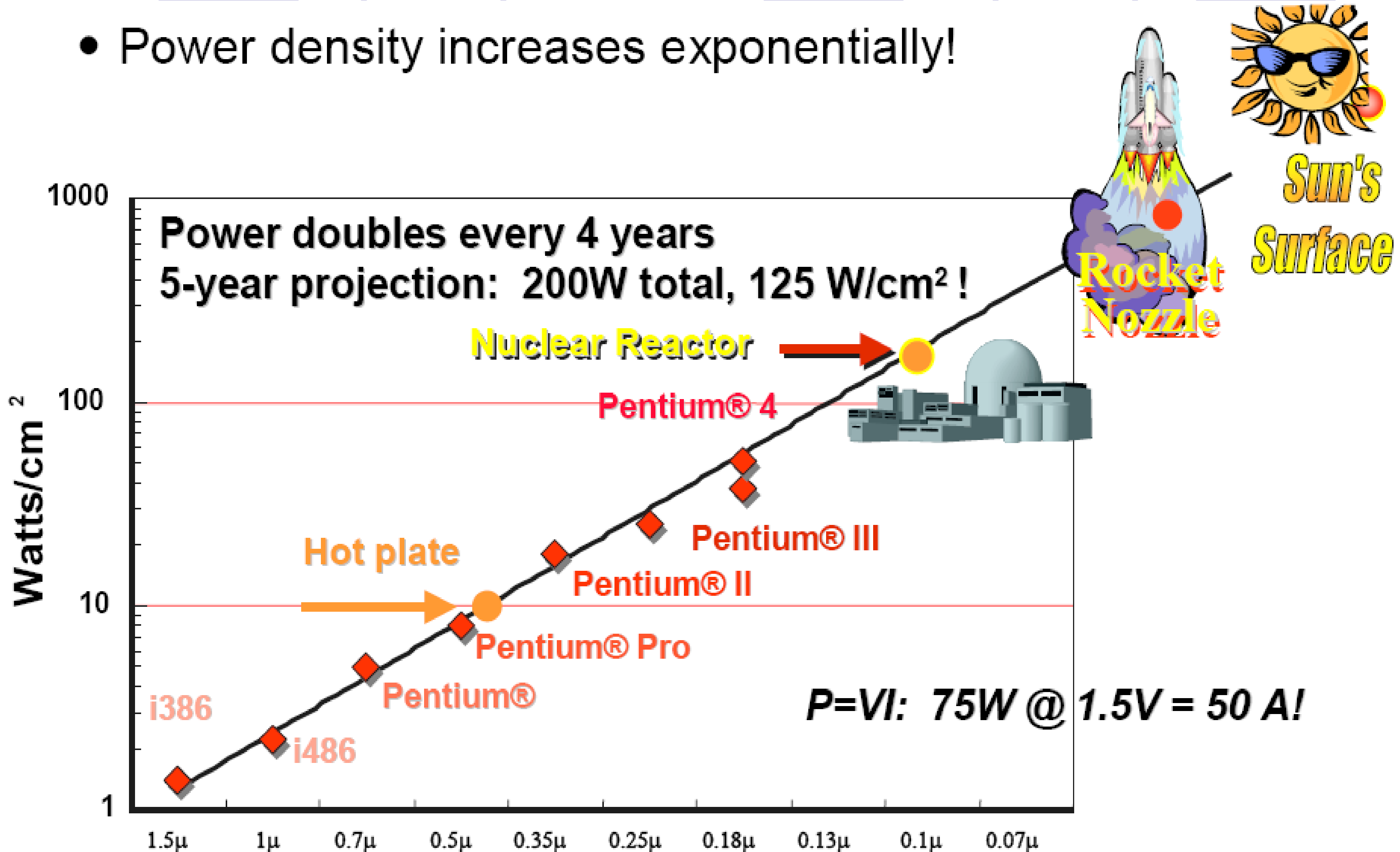


Problems with 10-layer metal?



Reliability Is Another Big Problem!!

- Power density increases exponentially!



Design Styles

- Specific design styles shall require specific CAD tools

Issues of VLSI circuits

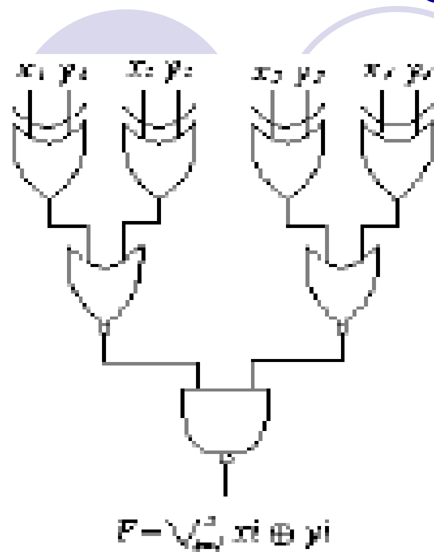
Performance | Area | Cost | Time–to–market

Different design styles

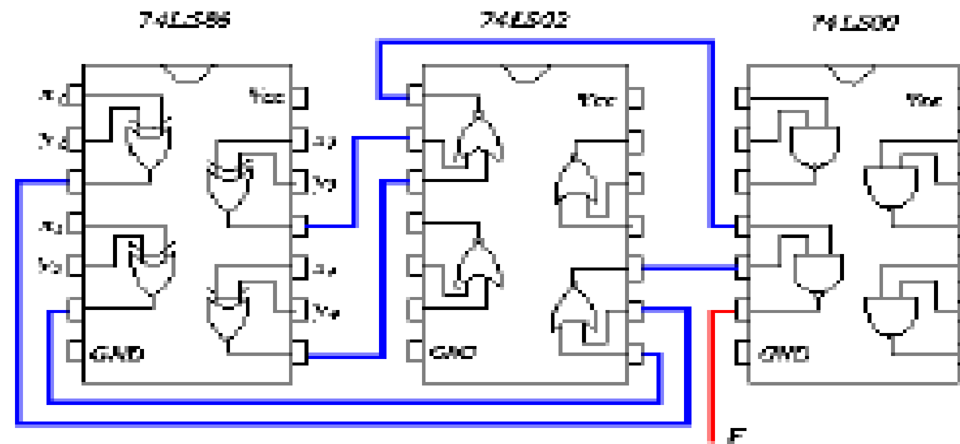
Full custom | Standard cell | Gate array | FPGA | *CPLD* | *SPLD* | *SSI*

Performance, Area efficiency, Cost, Flexibility

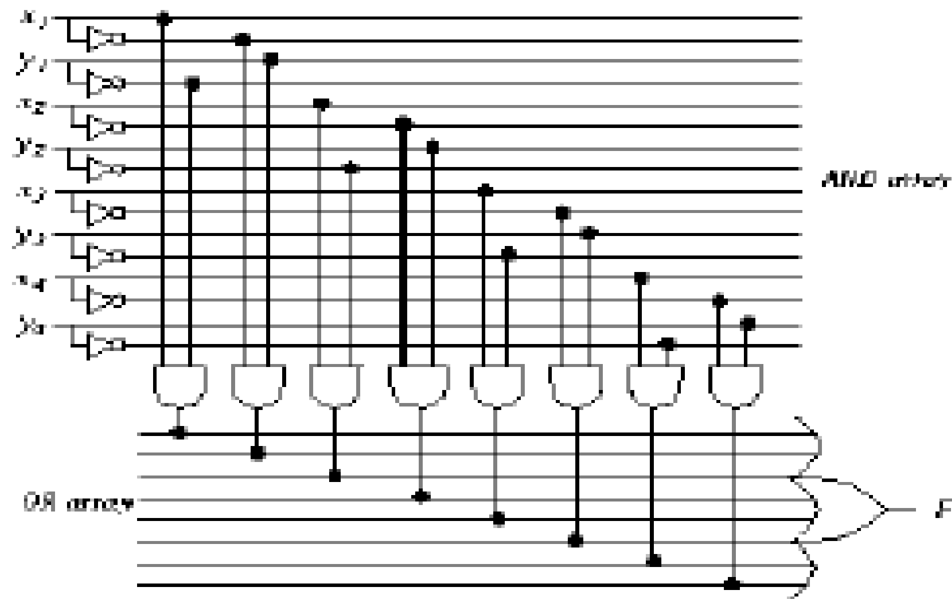
SSI/SPLD Design Style



(a) 4–bit comparator.



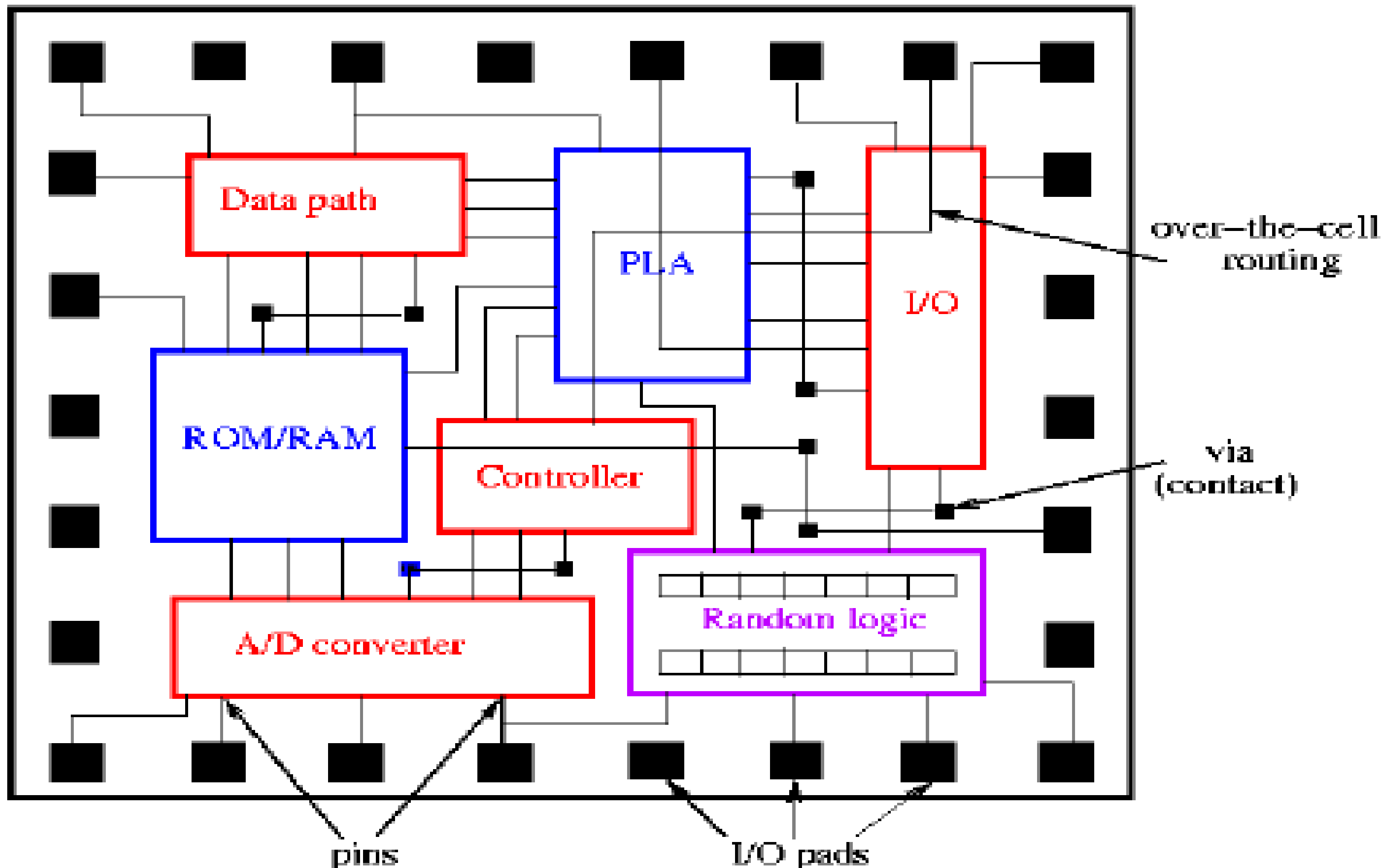
(b) SSI implementation.



(c) SPLD (PLA) implementation.

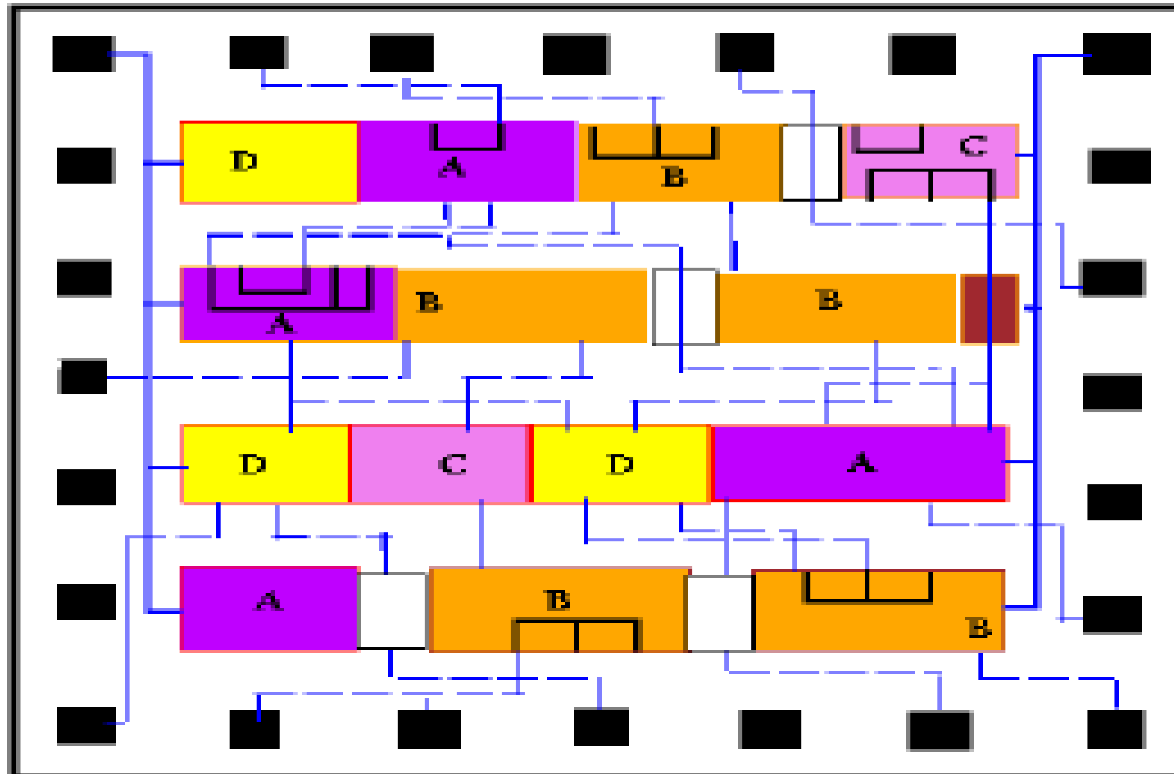
Full Custom Design Style

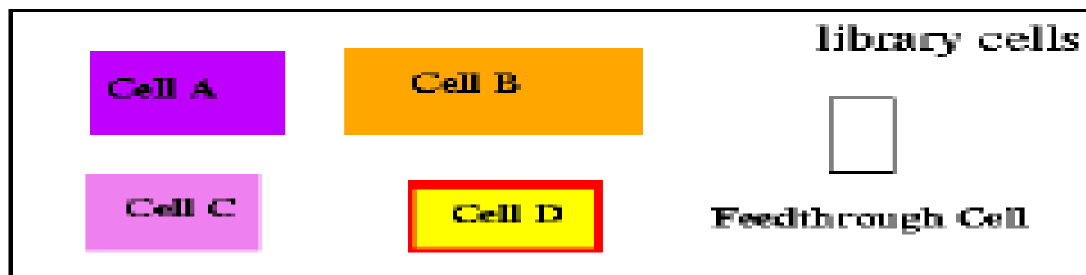
- Designers can control the shape of all mask patterns.
- Designers can specify the design up to the level of individual transistors.



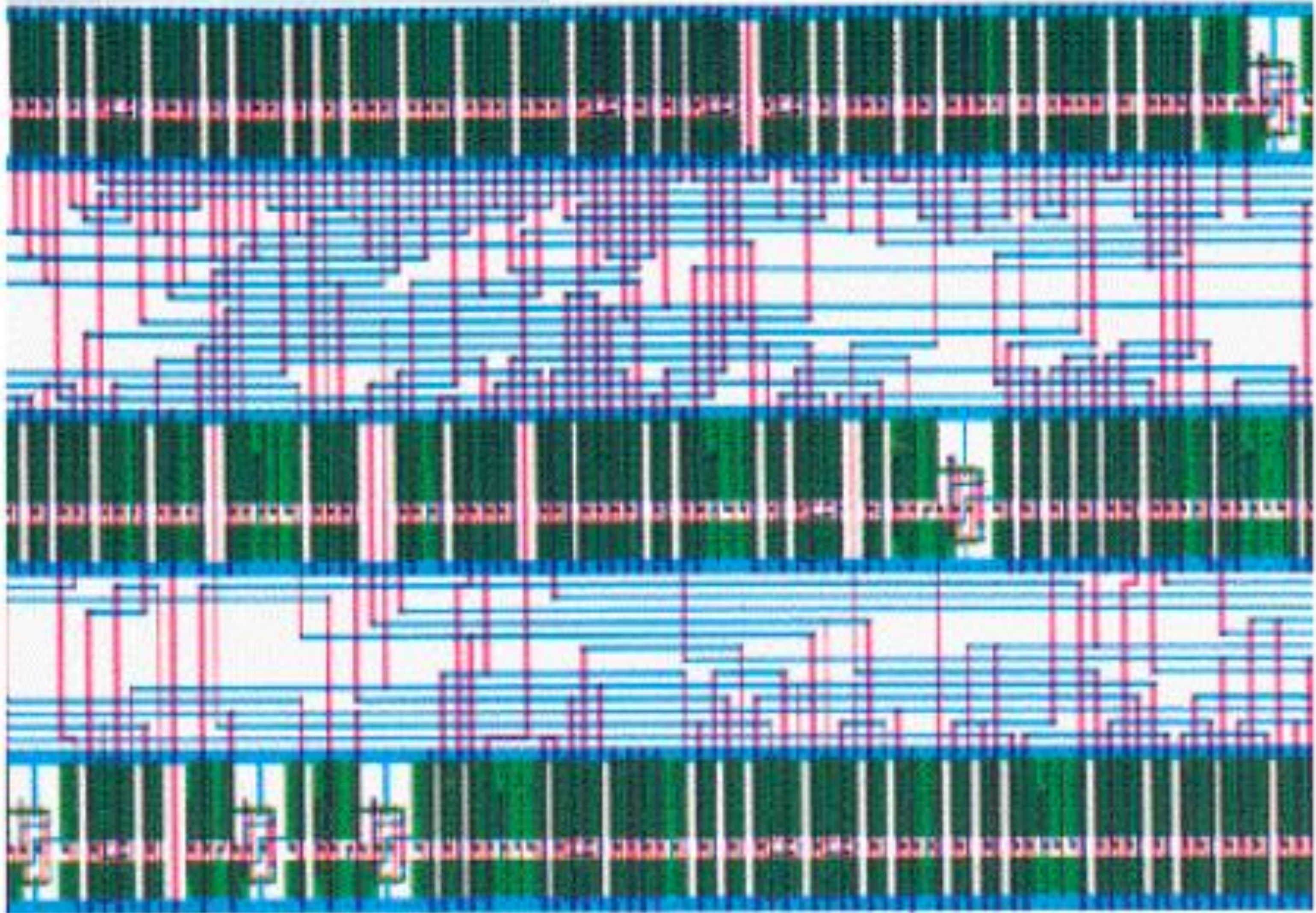
Standard Cell Design Style

• Selects pre-designed cells (of same height) to implement logic





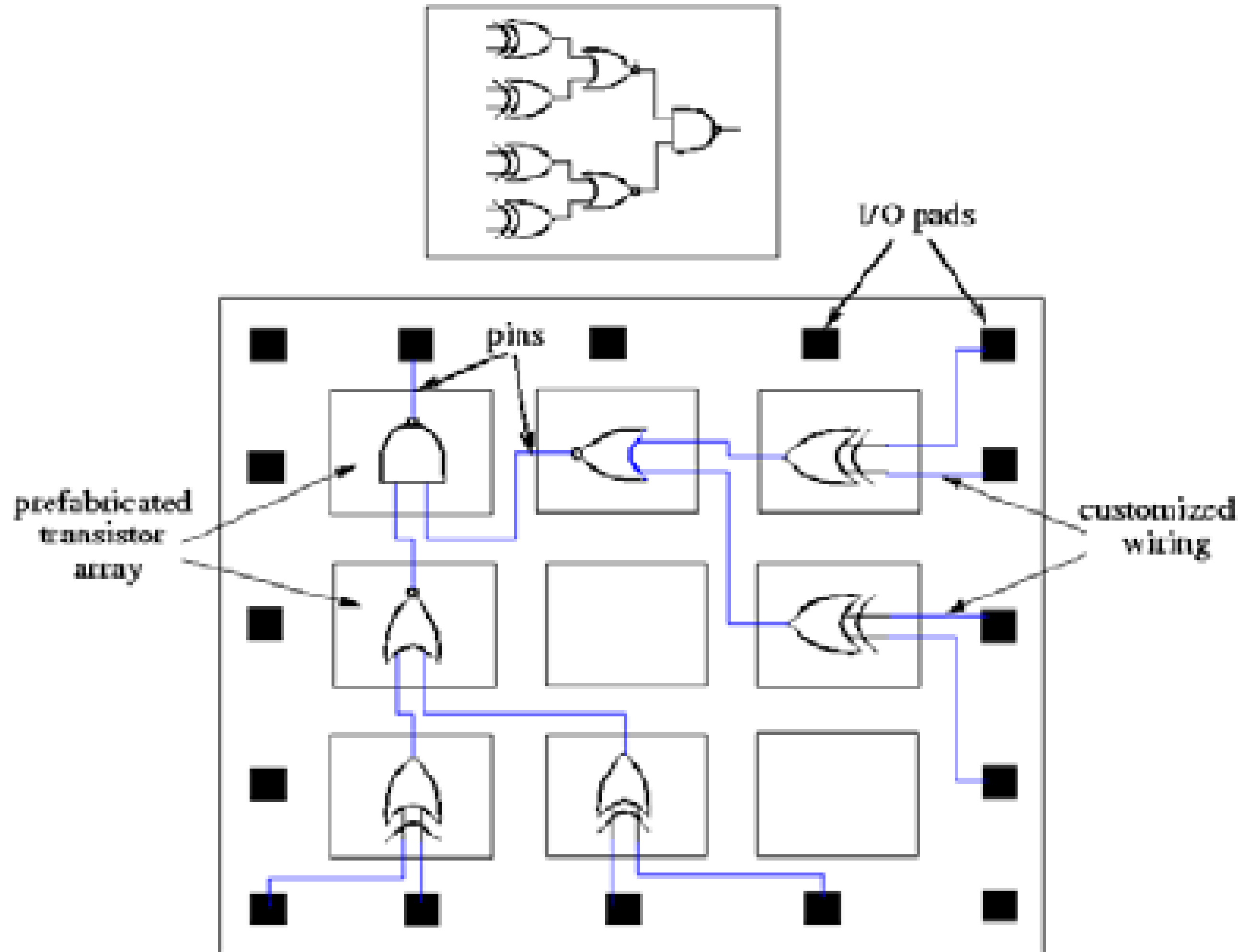
Standard Cell Example



Courtesy Newton/Pister, UC-Berkeley

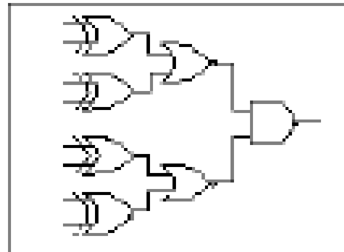
Gate Array Design Style

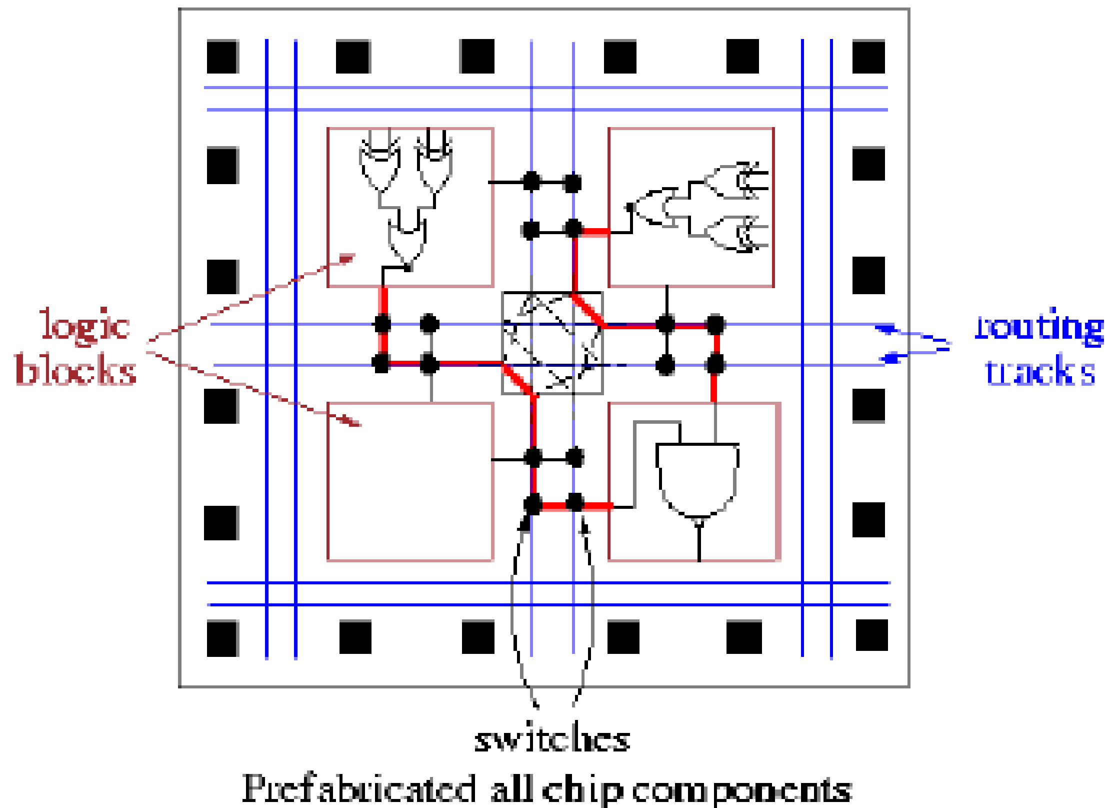
- Prefabricates a transistor array
- Needs wiring customization to implement logic



FPGA Design Style

- Logic and interconnects are both prefabricated.
- Illustrated by a symmetric array-based FPGA





Prefabricated all chip components

Comparisons of Design Styles

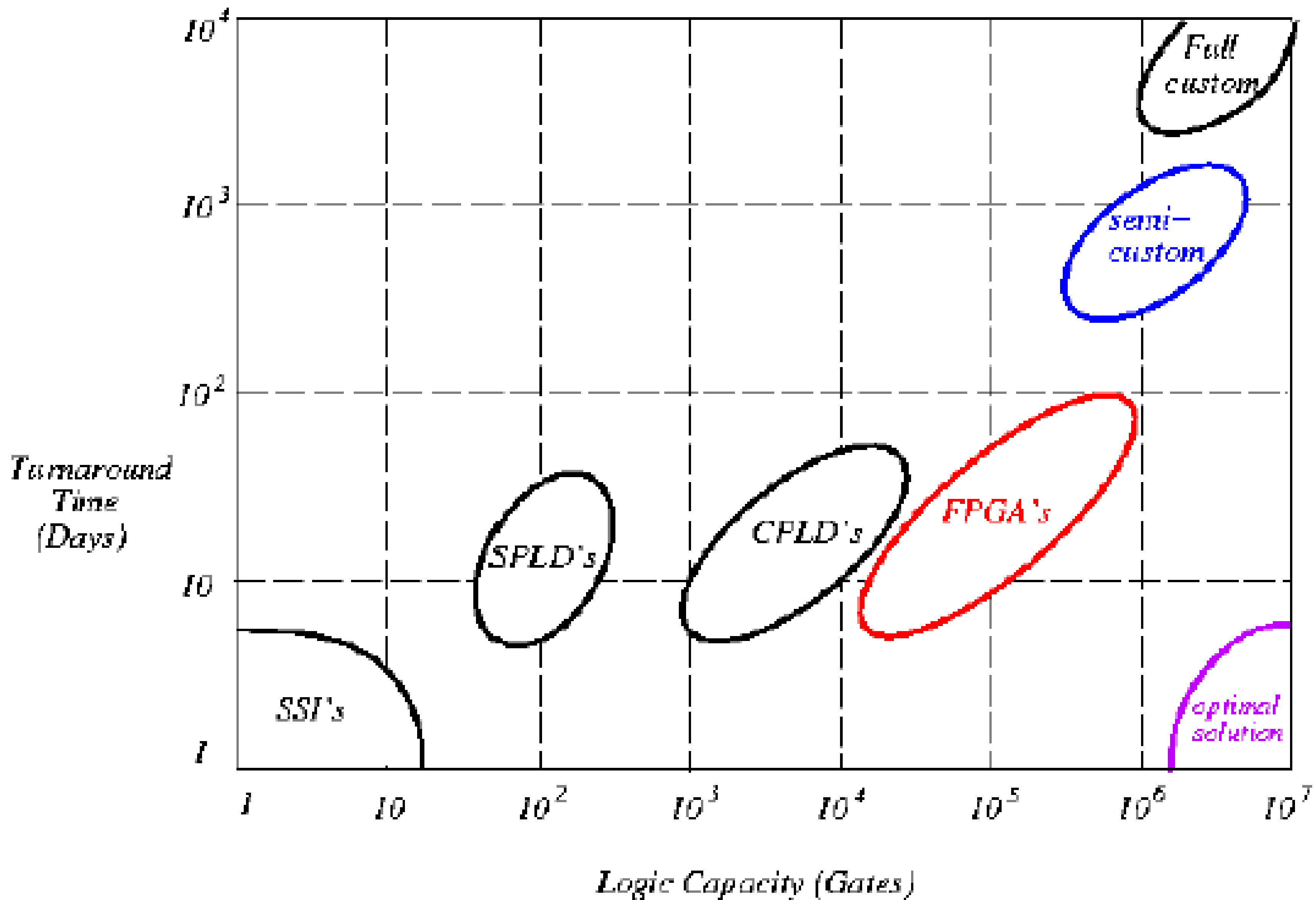
	Full custom	Standard cell	Gate array	FPGA	SPLD
Cell size	variable	fixed height*	fixed	fixed	fixed
Cell type	variable	variable	fixed	programmable	programmable
Cell placement	variable	in row	fixed	fixed	fixed
Interconnections	variable	variable	variable	programmable	programmable

* Uneven height cells are also used.

	Full custom	Standard cell	Gate array	FPGA	SPLD
Fabrication time	− − −	− −	+	+++	++
Packing density	+++	++	+	− −	− − −
Unit cost in large quantity	+++	++	+	− −	−
Unit cost in small quantity	− − −	− −	+	+++	++
Easy design and simulation	− − −	− −	−	++	+
Easy design change	− − −	− −	−	++	++
Accuracy of timing simulation	−	−	−	+	++
Chip speed	+++	++	+	−	− −

+ desirable; − not desirable

Design Style Trade-offs



Technology Roadmap for Semiconductors

Year	1997	1999	2002	2005	2008	2011	2014
Technology node (nm)	250	180	130	100	70	50	35
On-chip local clock (GHz)	0.75	1.25	2.1	3.5	6.0	10	16.9
Microprocessor chip size (mm^2)	300	340	430	520	620	750	901
Microprocessor transistors/chip	11M	21M	76M	200M	520M	1.40B	3.62B
Microprocessor cost/transistor ($\times 10^{-8}$ USD)	3000	1735	580	255	110	49	22
DRAM bits per chip	256M	1G	4G	16G	64G	256G	1T
Wiring level	6	6–7	7	7–8	8–9	9	10
Supply voltage (V)	1.8–2.5	1.5–1.8	1.2–1.5	0.9–1.2	0.6–0.9	0.5–0.6	0.37–0.42
Power (W)	70	90	130	160	170	175	183

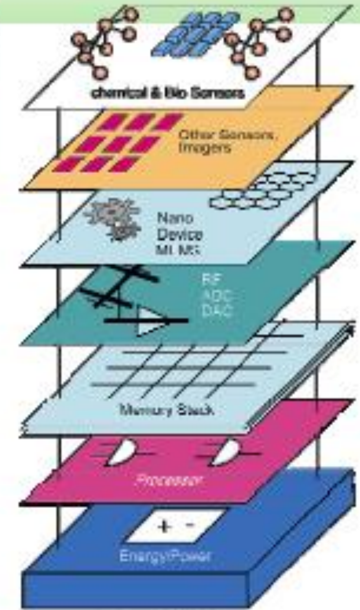
- Source: International Technology Roadmap for Semiconductors (ITRS), Nov. 2002. http://www.itrs.net/ntrs/publntrs.nsf.
- Deep submicron technology: node (**feature size**) < 0.25 μ*m*.
- Nanometer Technology: node < 0.1 μ*m*.

More Than Moore: 3D IC

Solid State Discrete Transistors

Planar (2-D) Integrated Circuits

3-D Integrated Circuits

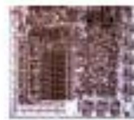


Heterogeneous Integration

1950s — 2000s — 2010s — 2020s

1 Transistor

16 Transistors



4500 Transistors

275,000 Transistors

3,100,000 Transistors

592,000,000 Transistors

>>1B transistors

Source: Fairchild, Intel & CS Tan(NTU-SG)

3D IC Design

- 3D IC technology is to stack multiple device layers into a monolithic chip.
- It has several advantages listed as follows:
  - Higher integration density: it can place more elements into one single package using much smaller area than a traditional 2D IC.
  - Heterogeneous integration: it can integrate disparate technologies, such as logic circuit, memory, and mixed signal components.
  - Higher performance: it can significantly reduce the wire-length.
  - Lower power: it can lower power consumption especially that for the clock net because of shorter wire-length.

3D IC Design

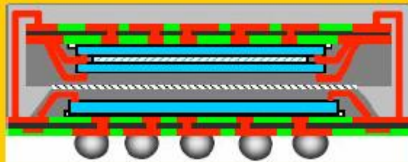
- Three kinds of fabrication technologies to implement 3D IC
  - **Package-on-Package** : it integrates packaged ICs into a new package.
  - **3D die stacking with wire bonding**: it integrates bare dice into the same package which are connected by wire bonding.
  - **3D IC integration with TSV**: it partitions integrated circuits into several dice and stacks the dice into a single package. Stack dice are connected by using through-silicon-vias (TSVs).

3D IC Design

3D Advanced Packaging

Package stacking

1. *PiP packages (Package in Package)*

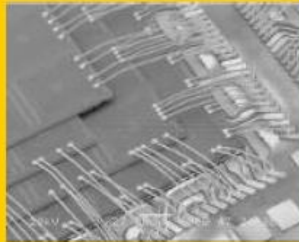


2. *PoP packages (Package on Package)*

→ *Rather OSATs*

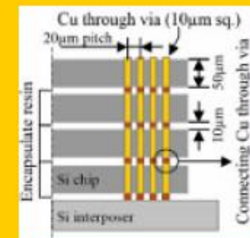
Die stacking

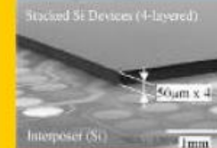
Wire Bonding



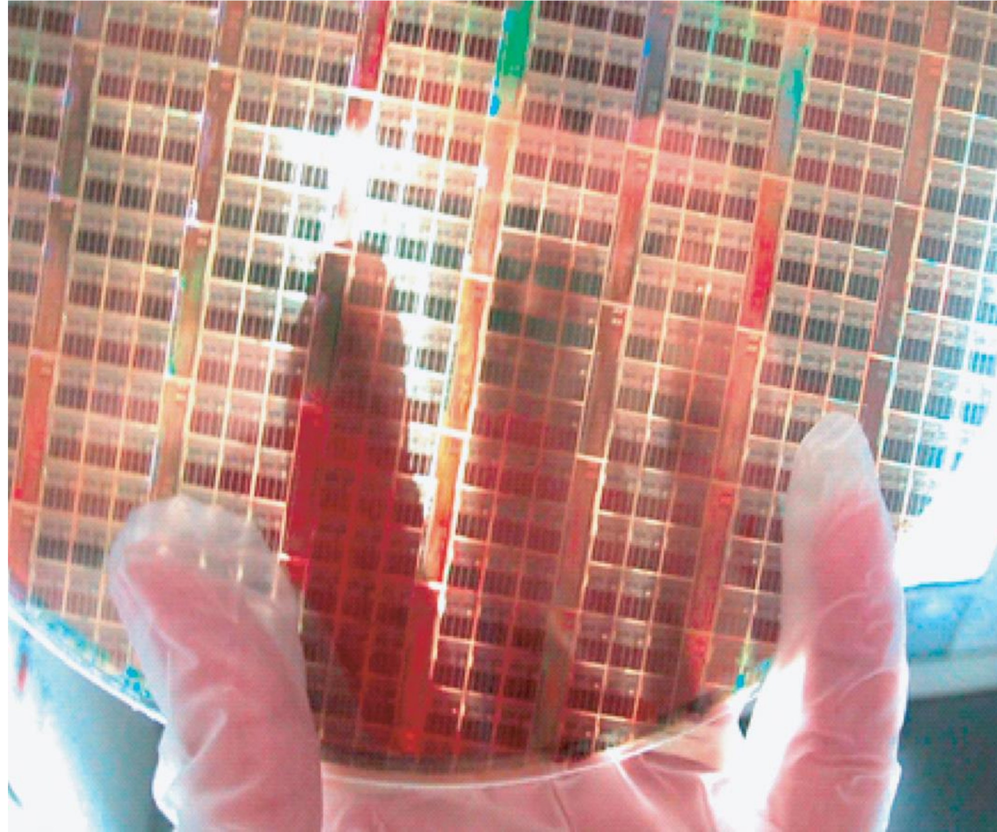
Wafer stacking

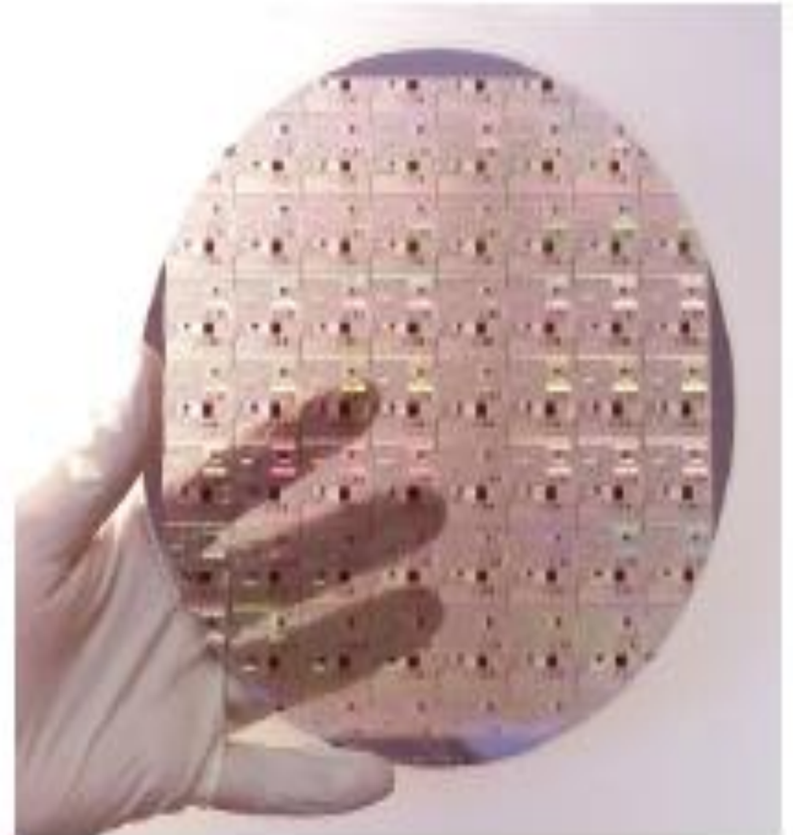
3D IC w/ TSV



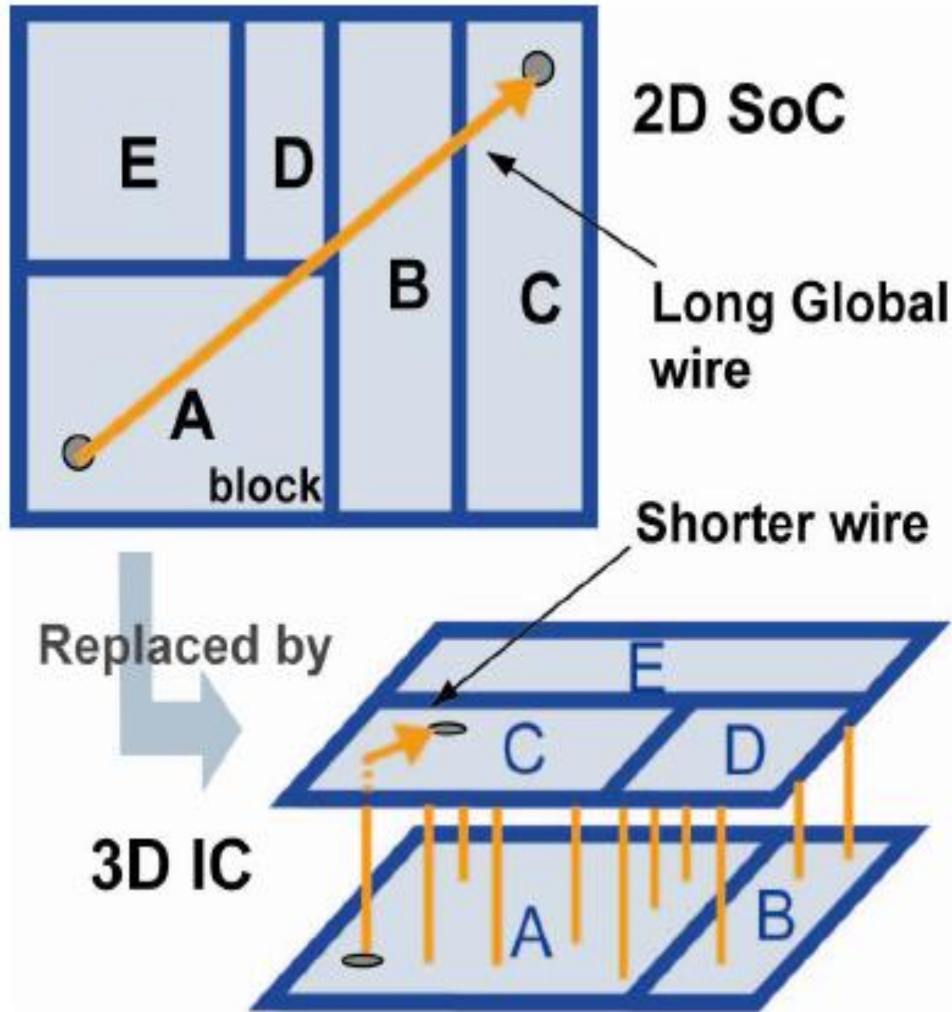


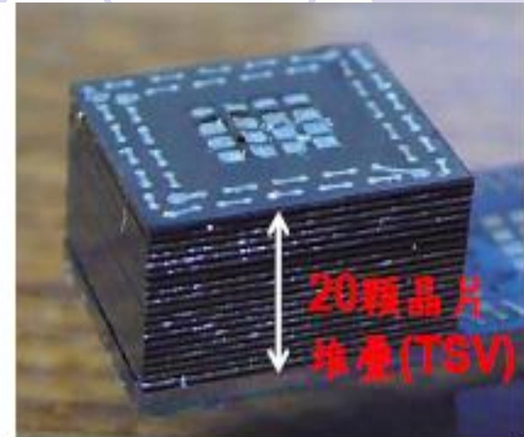
3D IC Design

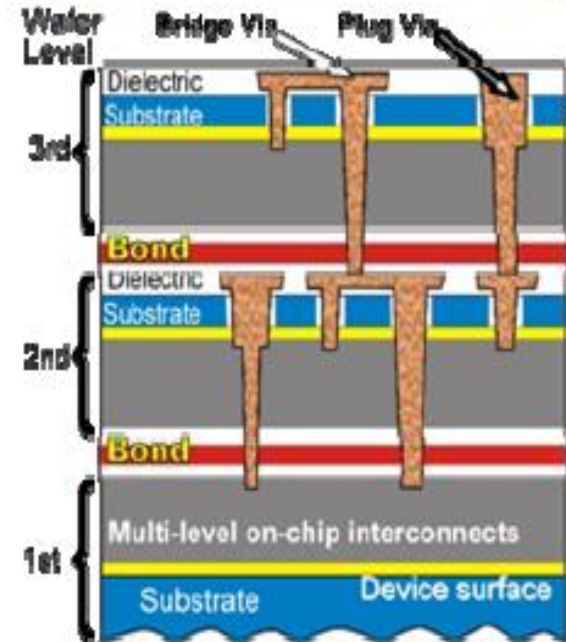




3D IC Design



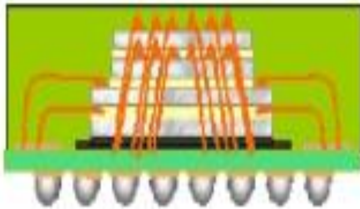




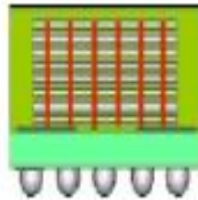
http://www.jonathassociates.com/AJA/droppedImage.png

3D IC Design

[Cross Section Comparison]

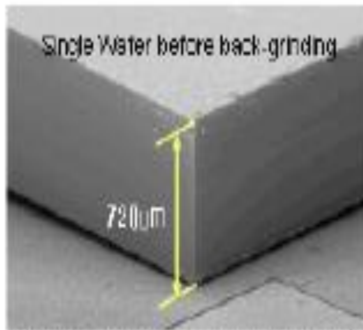


MCP Structure

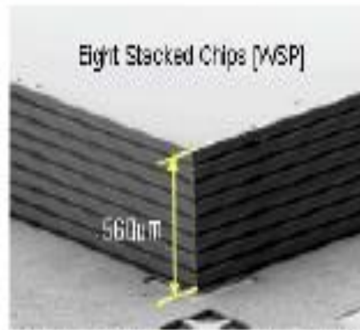


WSP Structure

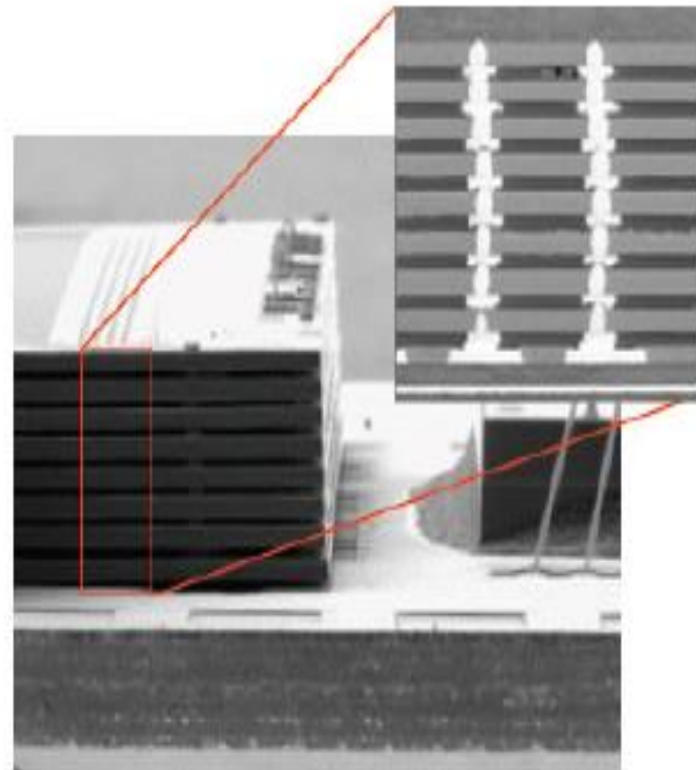
[Thickness Comparison]



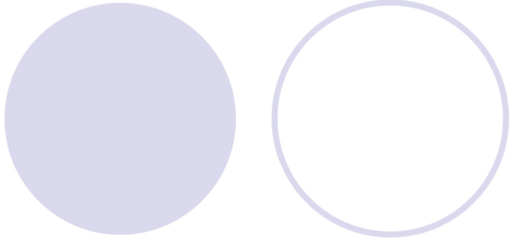
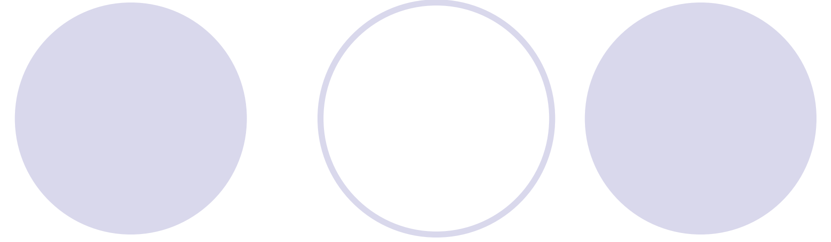
Single Wafer before Back-grinding



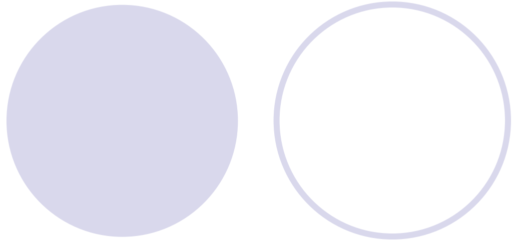
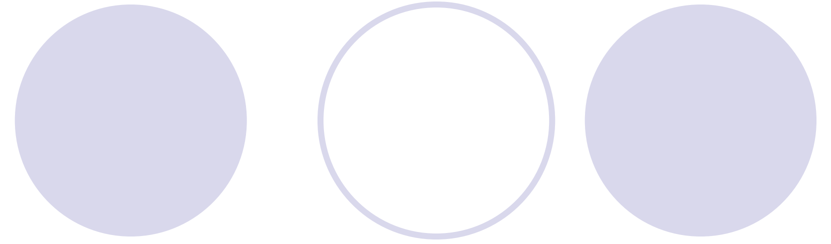
Eight-Chip WSP



Samsung 16Gb NAND stack with TSV

- Q&A

- Thanks for
- Your Attention