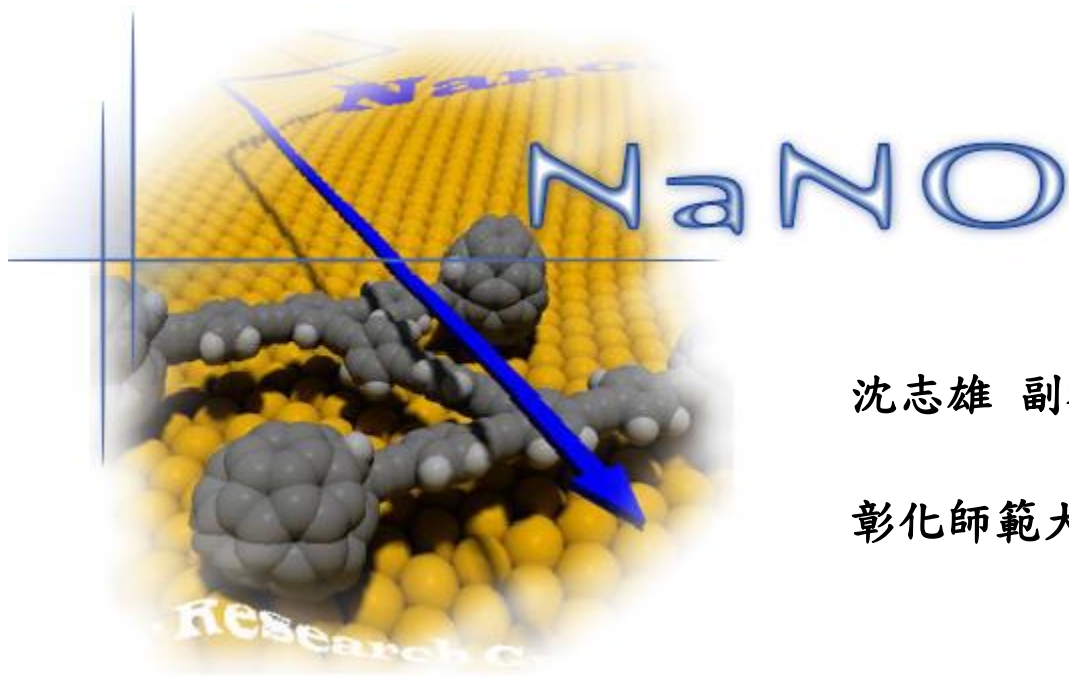




微小光機電的新科技生活



沈志雄 副教授

彰化師範大學機電工程學系



MOEMS



Contents

- **Macro**
- **Micro**
- **Matter**
- **Interaction**
- **Bottom Up**
- **Top Down**
- **What Happen ?**
- **Why Happen?**





章節



- 微光機電簡介
- 半導體工程
- 微機電工程
- CCD/ CMOS





Galaxy





世界是大還是小



科學家借助多種方法對英仙臂進行測量，有的認為有6 0 0 0多光年，有的說有1萬多光年，這一精確測量解決了長期爭論。



林肯號 大小：艦長約333公尺，甲板寬約77公尺

6000光年
= 5.4×10^{20} 公尺



金原子的直徑 0.3奈米

0.3 奈米
= 3×10^{-10} 公尺





What's NEW



你曾經有被繁複的化學結構式、分子式、各類鍵結、元素，弄得眼花撩亂、甚至上課想打退堂鼓的經驗嗎？希望這篇文章所報導的內容，能夠使你從一個嶄新的角度和態度，來發現其實學化學並沒有那麼困難。

美國德州萊斯大學的化學家James Tour，為了一項在中學裡推廣化學教育的計劃，採用了一種專業卻又不失新潮的方法。他的研究小組，透過組合不同的有機分子，合成稱為奈米娃娃(NanoKids)的分子結構。這些奈米娃娃，是在其整體分子結構上，酷似人的形狀(具有頭部、軀體、四肢)。這個方法的動機，是James Tour有鑒於一般人一看到化學結構就頭大，他就想何不利用類似兒童玩具的結構，來介紹化學鍵結、分子結構等觀念。

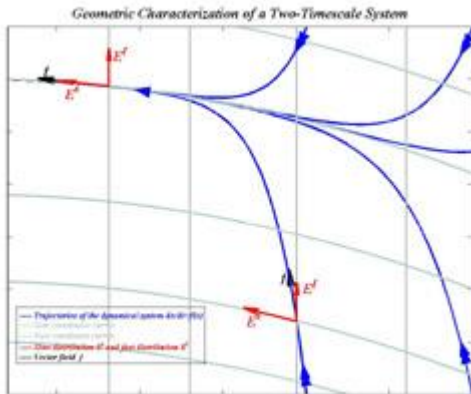
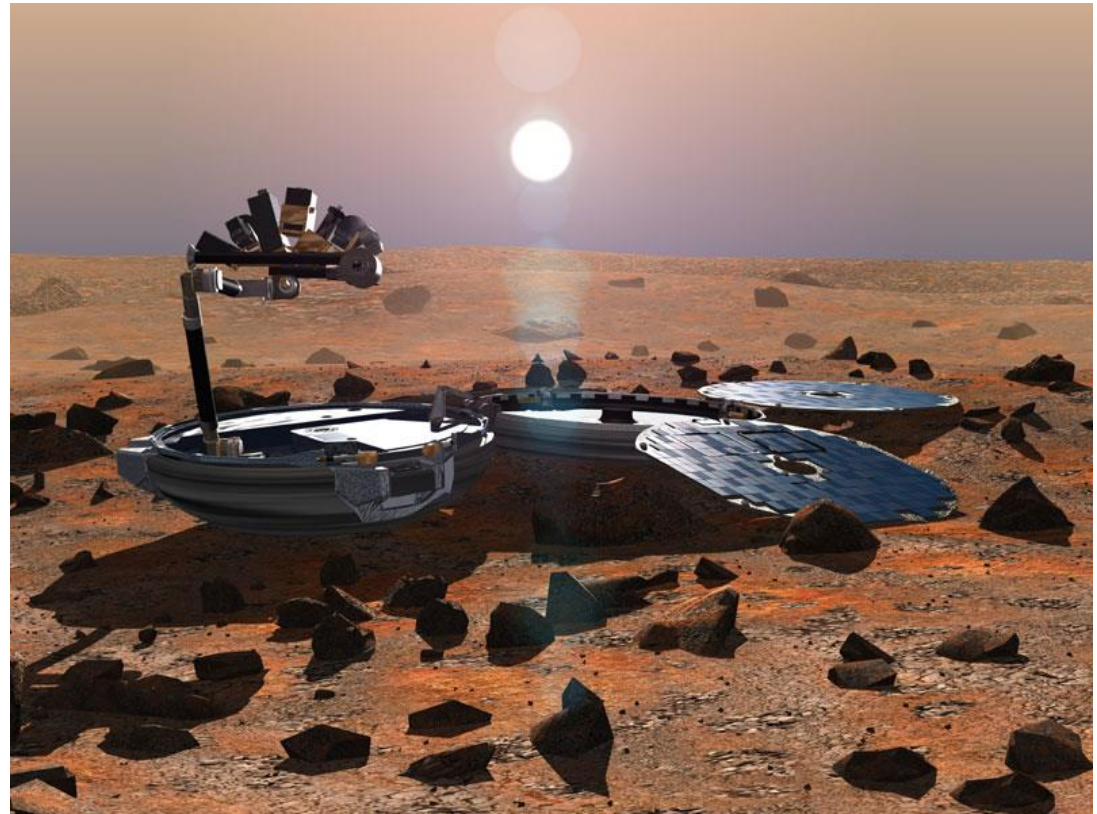
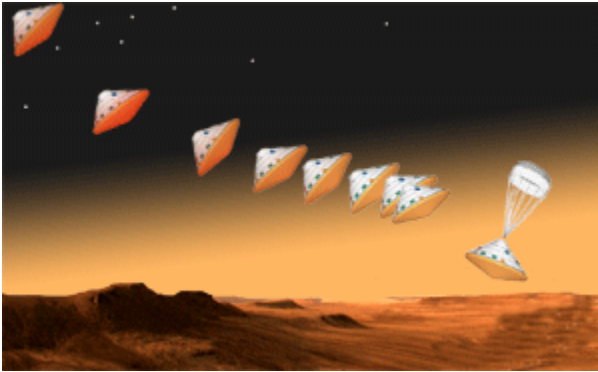
這些奈米娃娃的身體部份，是由苯環所組成。而由烷基等碳氫有機分子所組成的四肢，則是透過碘化物連接在身體上。至於娃娃的頭部，則是由醇類分子所構成。第一個奈米娃娃，是在2001年五月份”誕生”的。如果在這些奈米娃娃的足部加上硫，則可以使它們站立在鍍有金的表面。到目前為止，經過一些化學上的技巧，James Tour已經組成了一個包含胖嘟嘟的奈米寶寶(NanoKid)、留著一頭黃色長髮的奈米青少年(NanoTeen)、奈米綠扁帽(NanoGreenBeret)、奈米麵包師傅(NanoBaker)、奈米小丑(NanoJester)、奈米國王(NanoMonarch)、奈米主廚(NanoChef)、奈米清教徒(NanoPilgrim)、奈米德州佬(NanoTexan)、以及奈米學究(NanoScholar)等成員的”奈米家庭”。

<http://pubs.acs.org/cen/education/8214/8214nanokids.html>





Macro Engineering

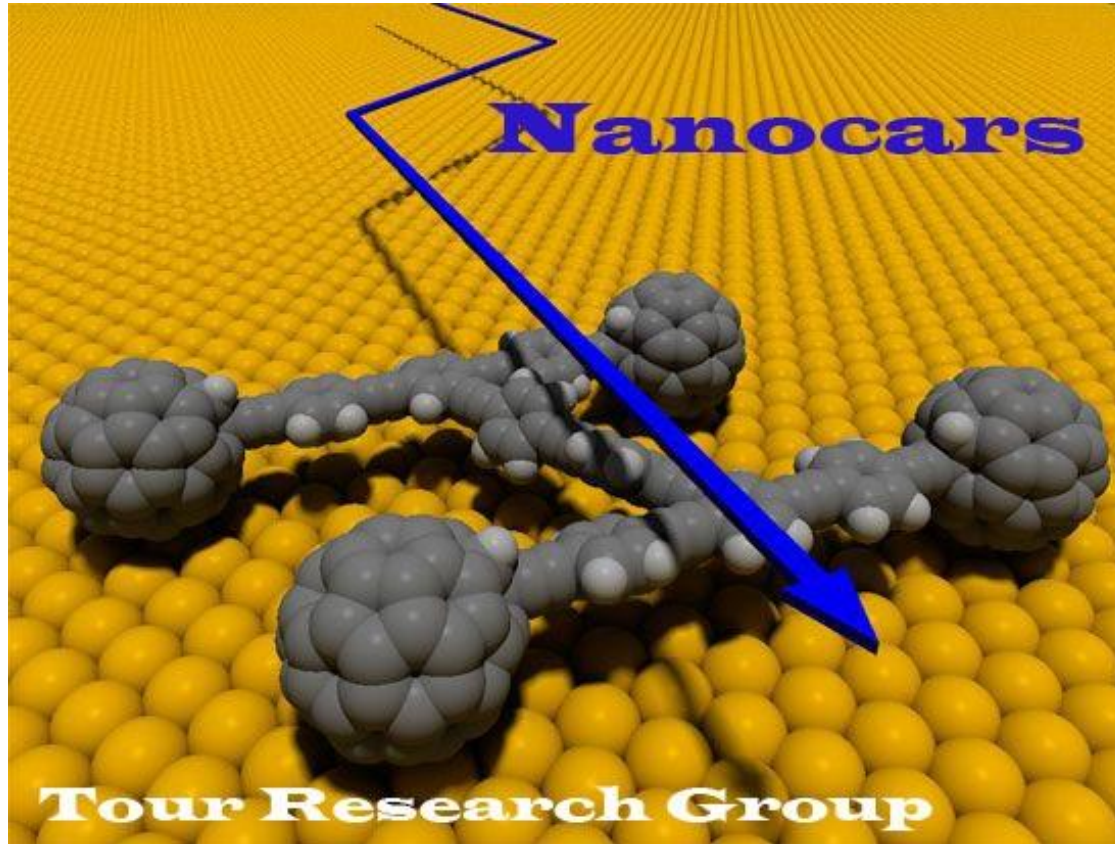


<http://www.nasa.gov/multimedia/videogallery/index.html>





Micro Engineering



MOEMS



T4 病毒入侵細菌動畫

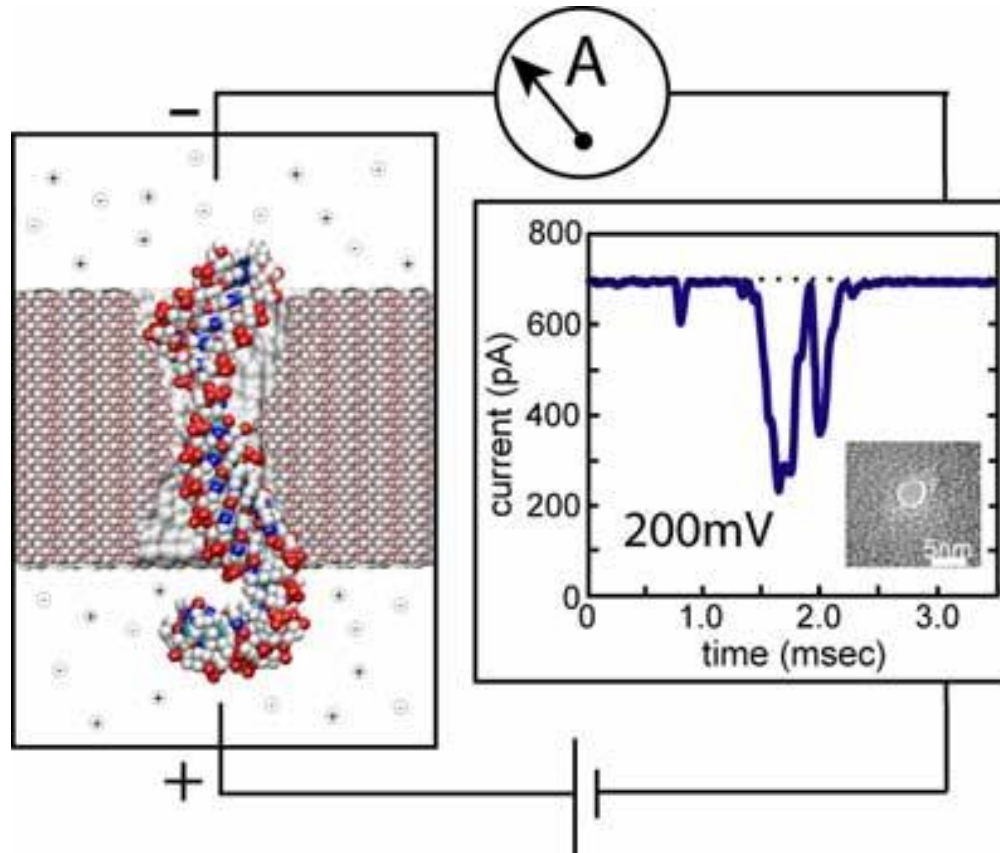


各大科學期刊競相報道的高清晰T4病毒入侵細菌動畫，製作非常精美，美俄日三國科學家共同完成，刊登於04年8月20日出版的《Cell》雜誌上。





Translocation of DNA through Synthetic Nanopores



<http://www.ks.uiuc.edu/Gallery/Movies/>





微光機電簡介

光機電系統整合

Courtesy of D. Thomas, Perkin-Elmer Applied Biosystems

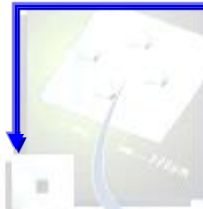
Inertial Navigation Sensors
 • Acceleration
 • Yaw Rate

Silicon Nozzles for Fuel Injection

Micromachined Transducer
 Applications for Automotive Operation & Safety

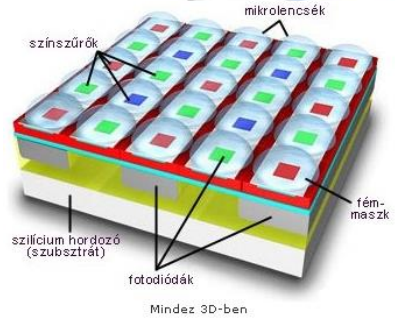
Micromachined Accelerometer for Airbag

Airbag



Micromachined Transducer

Standard Tire Pressure



半導體

Process

微機電元件

光機

Tire Pressure Sensors

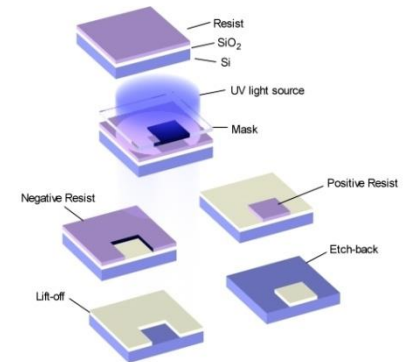
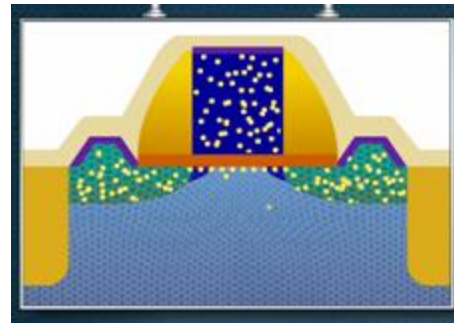
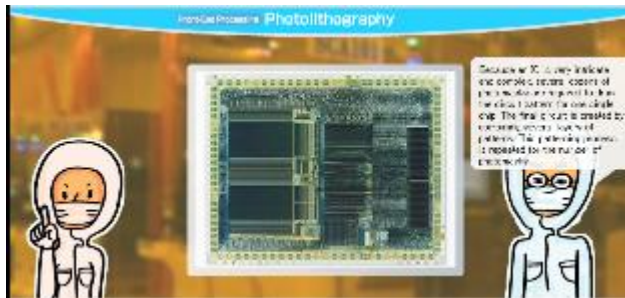


MOEMS



半導體工程

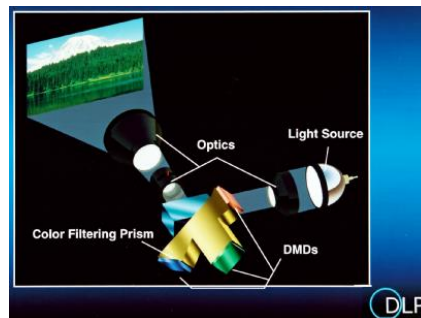
- 半導體製程技術：NEC、美國應材
- 微影、蝕刻





微機電工程

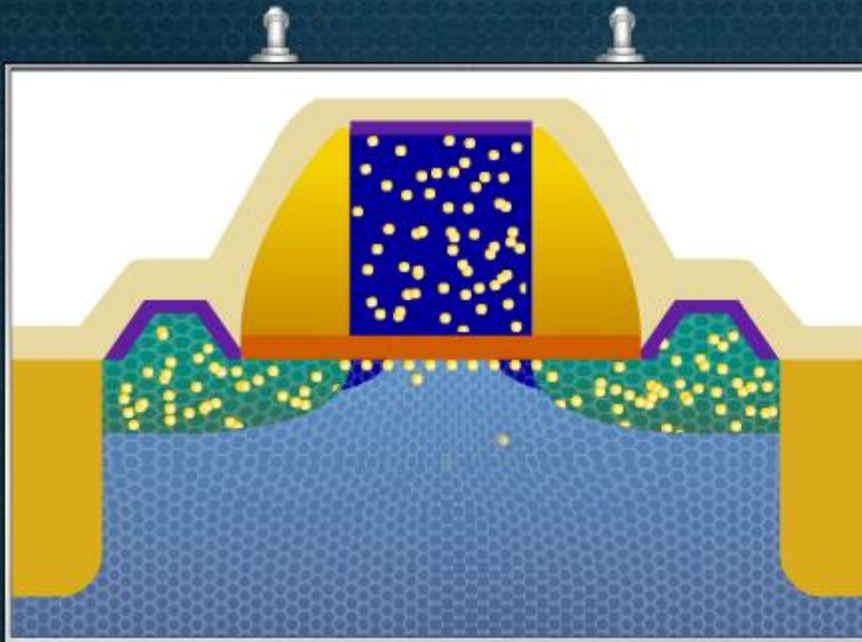
- Wii 加速計
- DLP 投影機



MOEMS



Top Down Nano Device



RUN FAST SCORE: **29**
STAY COOL SCORE: **46**

TOTAL SCORE: 75

SPEED: Not bad, a little more practice and your device will be humming.

TEMP: You're staying cool, but it wouldn't hurt to optimize.

Want to optimize your device for better performance ...and a higher score?

PERFORMANCE ANALYSIS



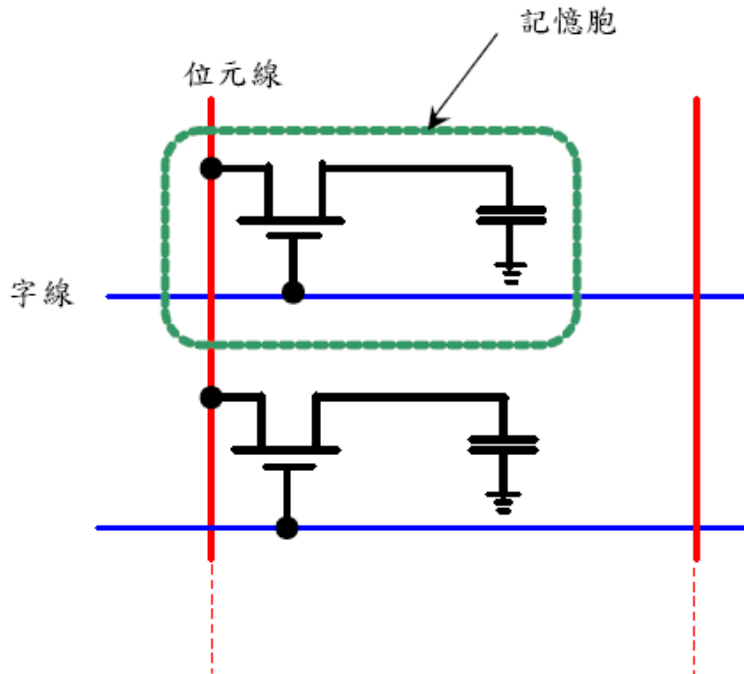
Would you like to optimize your device?

OPTIMIZE

NO, THANKS



DRAM原理



DRAM 的記憶胞基本上就是一個電容加上一個控制充放電及讀取的電晶體開關。這裡用的是NMOS，但是源極和汲極並沒特別標出，主要原因是他是用作雙向開關，電流可以流入或流出電容。

每一個記憶胞會外接兩條線，一條是控制閘極的稱字線(word line)，加上正電壓時可以選擇同一行的記憶胞（同一個字的不同位元），將他們的NMOS 開關導通；另一條接到源/汲極的稱為位元線(bit line)，用來”寫”或”讀”資料到記憶胞中。

DRAM 架構

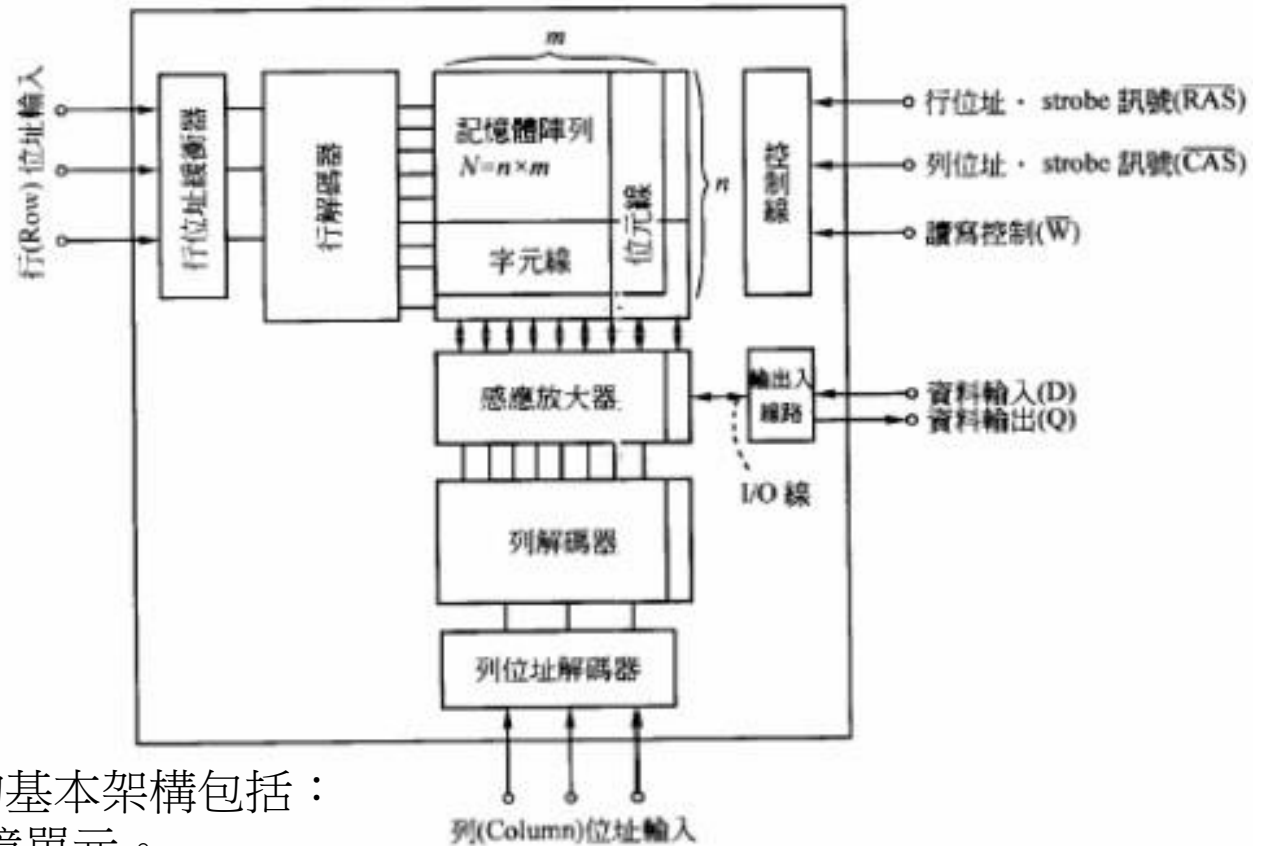
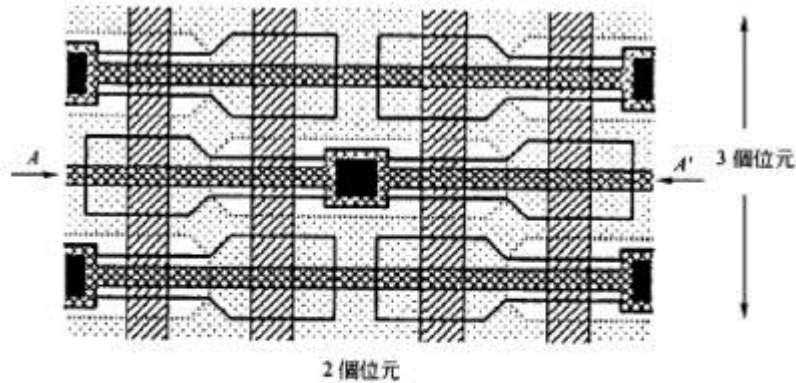


圖-1 MOS DRAM 的結構

根據以上的介紹DRAM的基本架構包括：

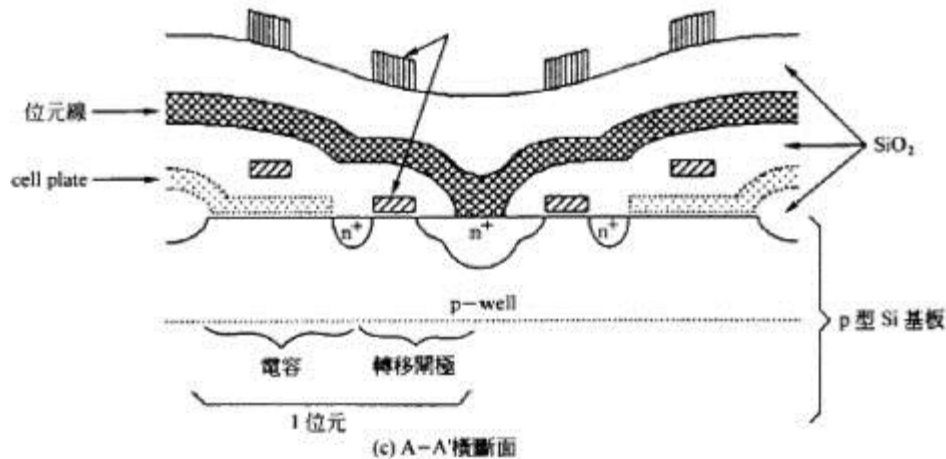
- 排列成二次元陣列的記憶單元。
- 感應放大器。
- 位址緩衝器(行/列)及位址解碼器(行和列)。
- 輸出預放大器、輸出主放大器和輸入緩衝器等輸出線路。
- 控制線路等

結構與佈局圖



(b) 平面圖(省略 A1 導線)

- | | | |
|------------|----------|--------------------|
| : field 區域 | : poly I | : poly II |
| : poly III | : A1 導線 | : poly III contact |



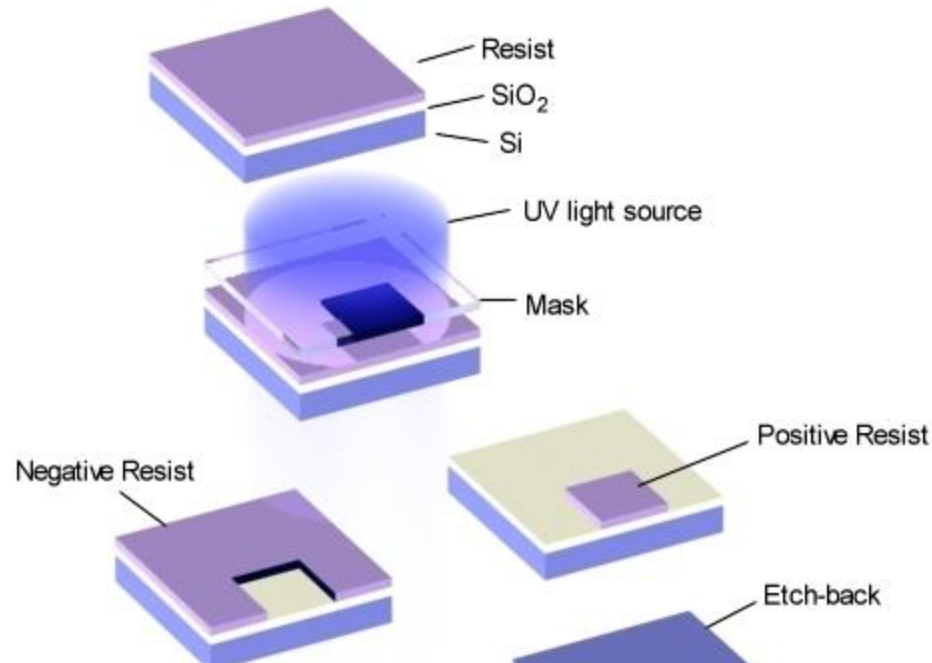
(c) A-A' 橫斷面

圖-2 1 電晶體 + 1 電容型的記憶單元

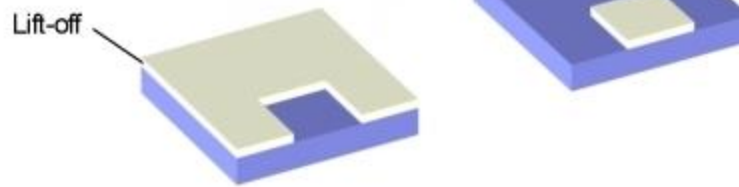


曝光顯影以及蝕刻

曝光顯影



蝕刻



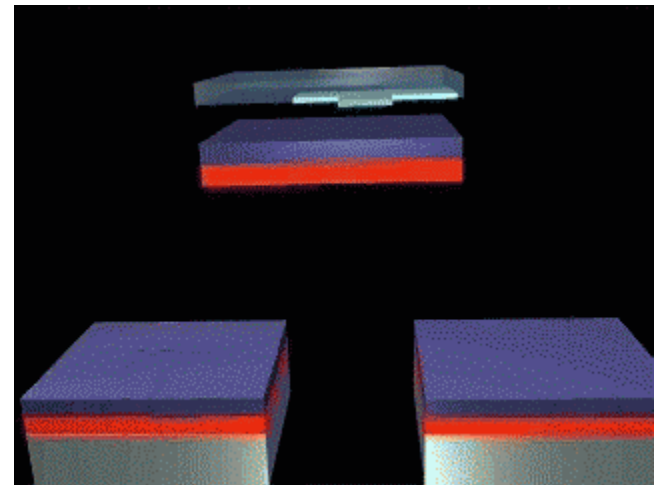


光罩

光罩即是將我們所要之設計電路圖形，利用電子束曝光系統將鉻膜上圖形製作在玻璃或石英上，再利用此光罩上金屬鉻膜擋住光線，而沒有金屬鉻膜的地方，光線就會穿透玻璃到達已塗佈有機光阻的晶圓上，經由光罩上透光與不透光的差別，可在光阻塗層上定義出曝光及不曝光的區域，經由適當的顯影步驟，去除感光的光阻（或去除未感光的光阻），即可用未感光的光阻（或感光的光阻），定義出光罩電路圖形。而目前晶圓上的光阻圖樣一般為光罩圖形的四分之一倍。

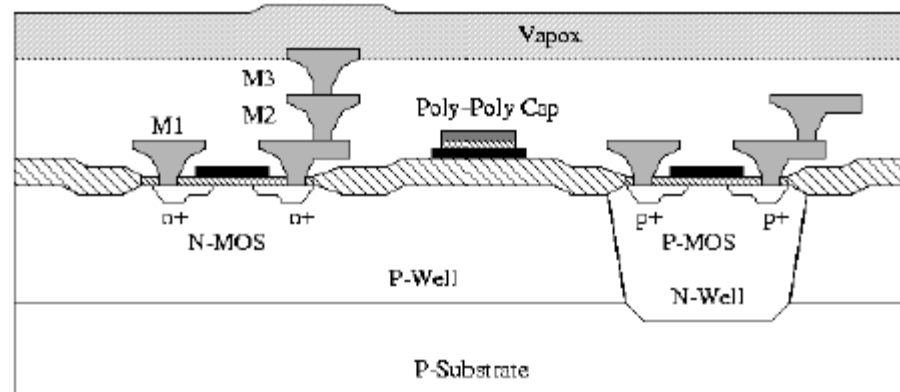


- 光阻介紹
- 光阻的作用是要將積體電路結構圖形印製在晶圓表面上，其功能有些類似底片上的感光劑。光阻主要可分為正光阻及負光阻二種。正光阻就是被光照射的部份可以被顯影液去除掉，而未曝光的光阻則不會被顯影液去除（左邊）。而負光阻則相反，被光照射的部份不會被顯影液去除，而其餘不被光所照射的區域將會被顯影液所去除（右邊）。

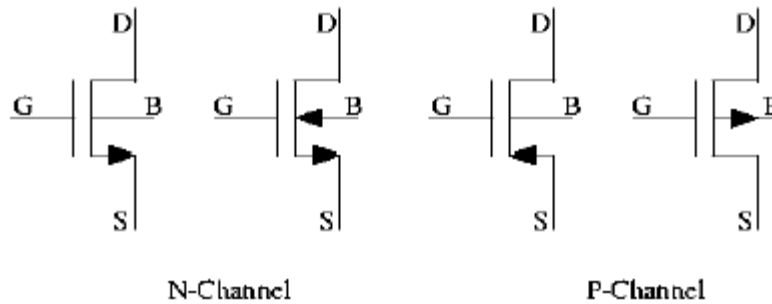




Characteristics of MOS Device



Symbols of the MOS transistors





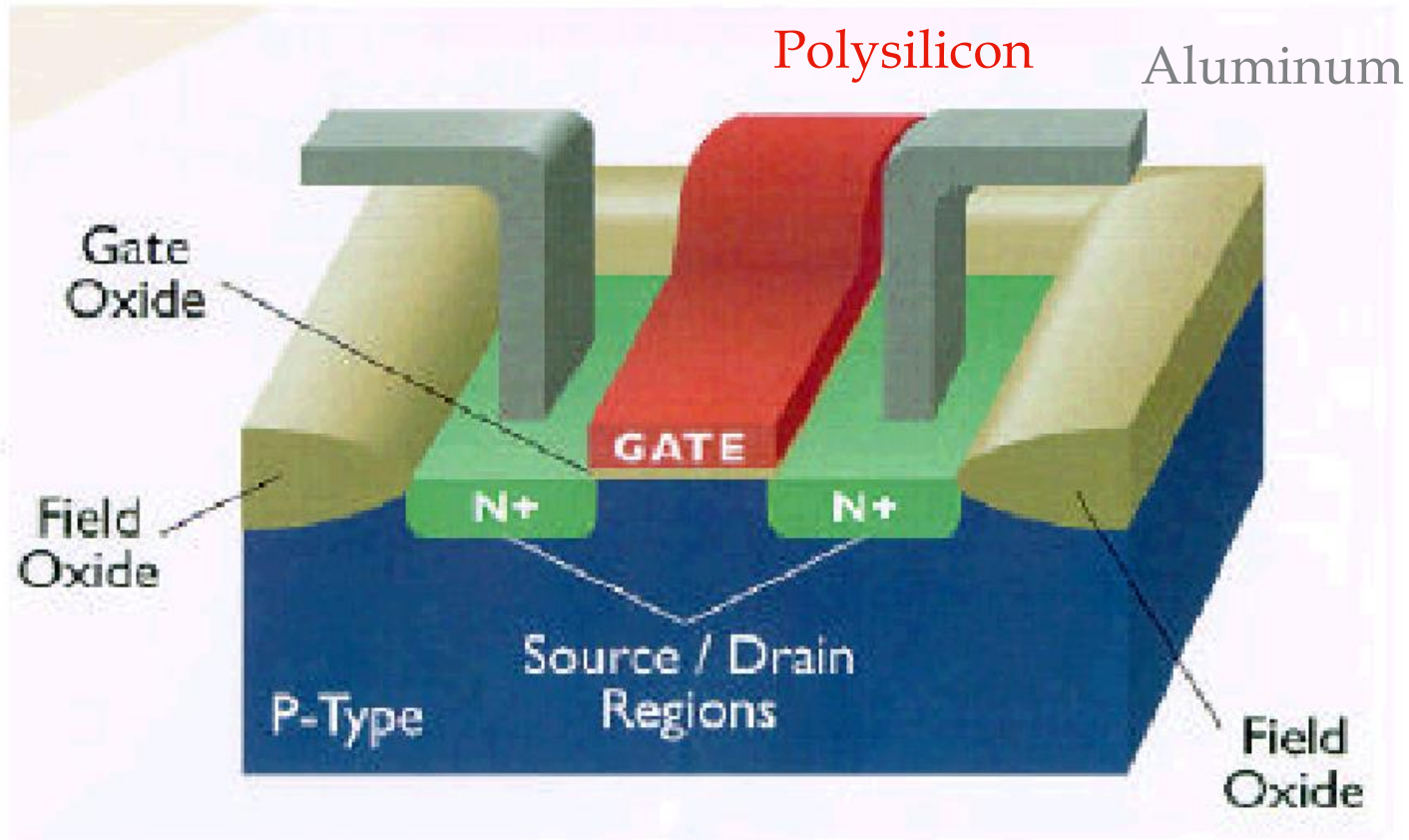
Design Rules



MOEMS



3D Perspective






Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
 - scalable design rules: lambda parameter
 - absolute dimensions (micron rules)









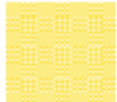













CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	





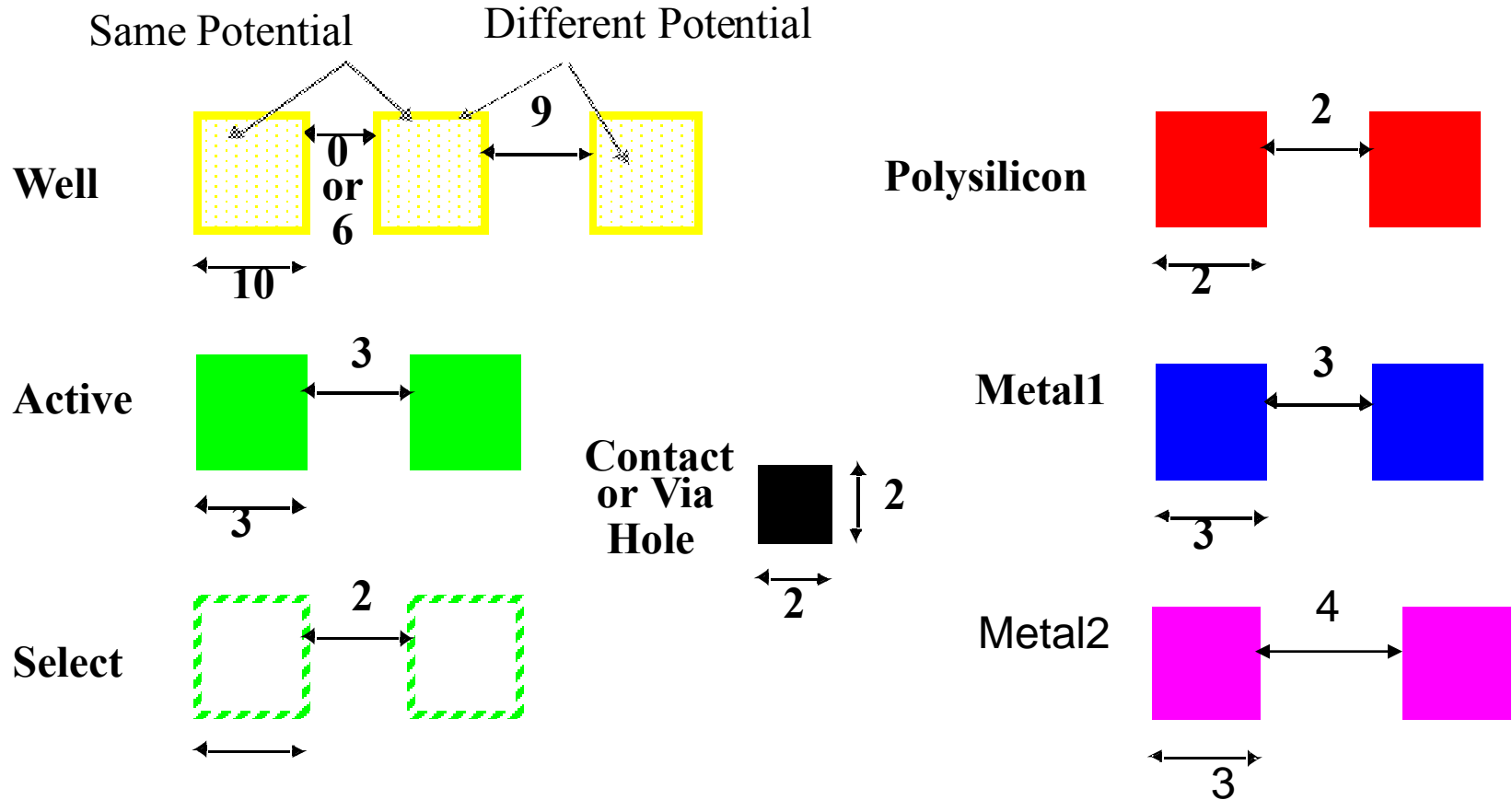
Layers in 0.25 μm CMOS process

Layer Description	Representation				
metal	 m1	 m2	 m3	 m4	 m5
well	 nw				
polysilicon	 poly				
contacts & vias	 ct	 v12,v23,v34,v45	 nwc	 pwc	
active area and FETs	 ndif	 pdif	 nfet	 pfet	
select	 nplus	 pplus	 prb		





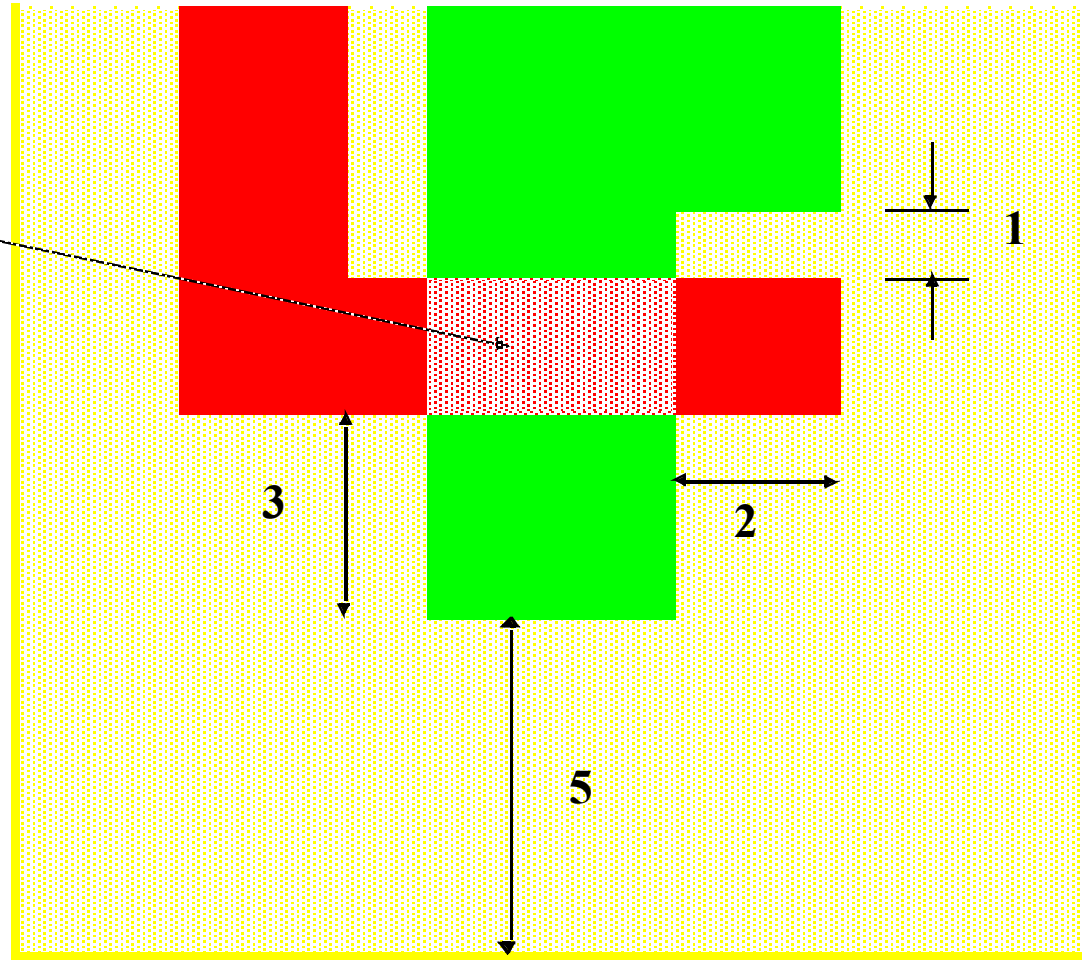
Intra-Layer Design Rules





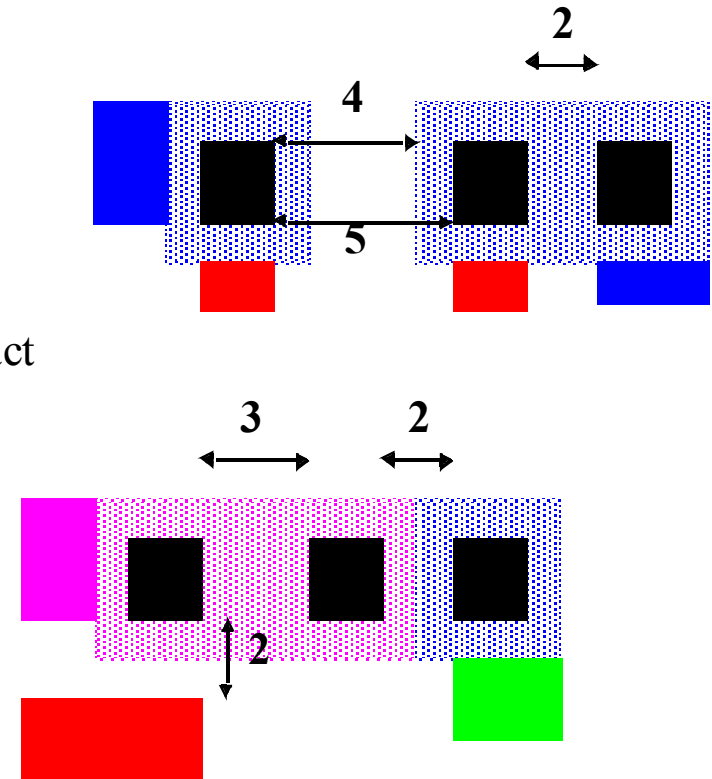
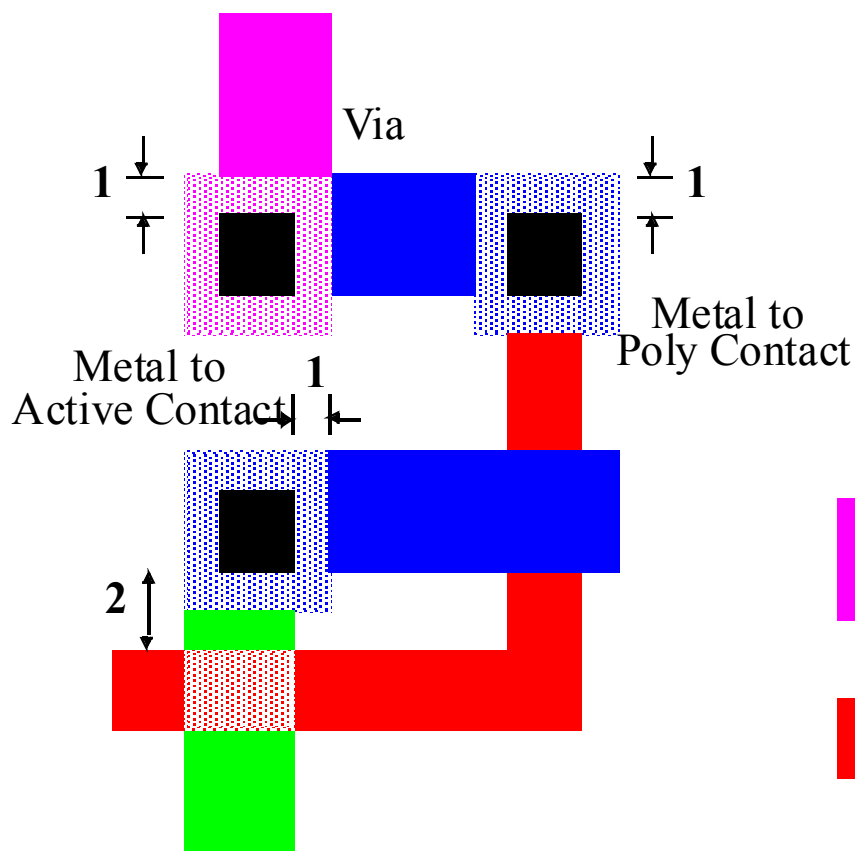
Transistor Layout

Transistor



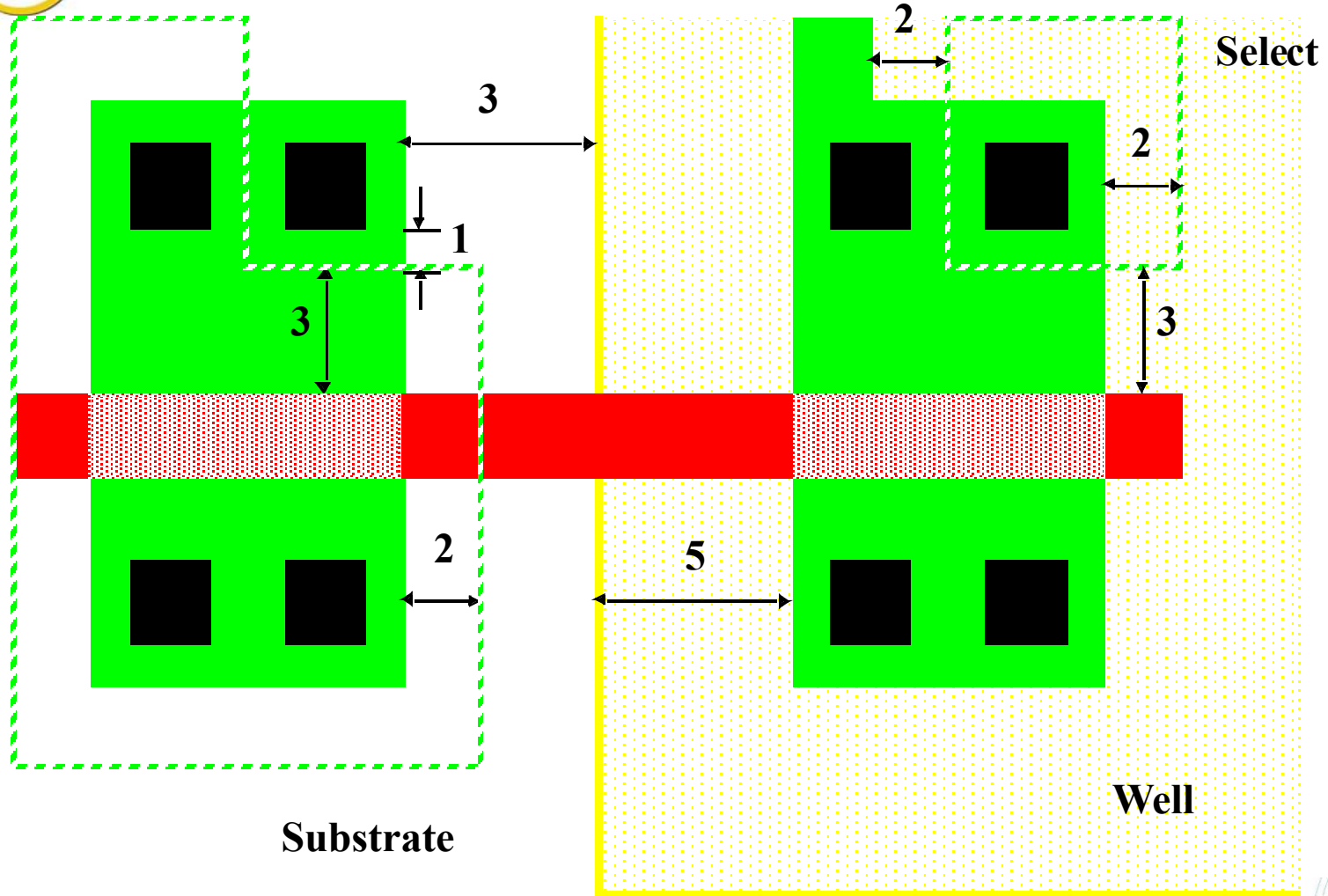


Vias and Contacts



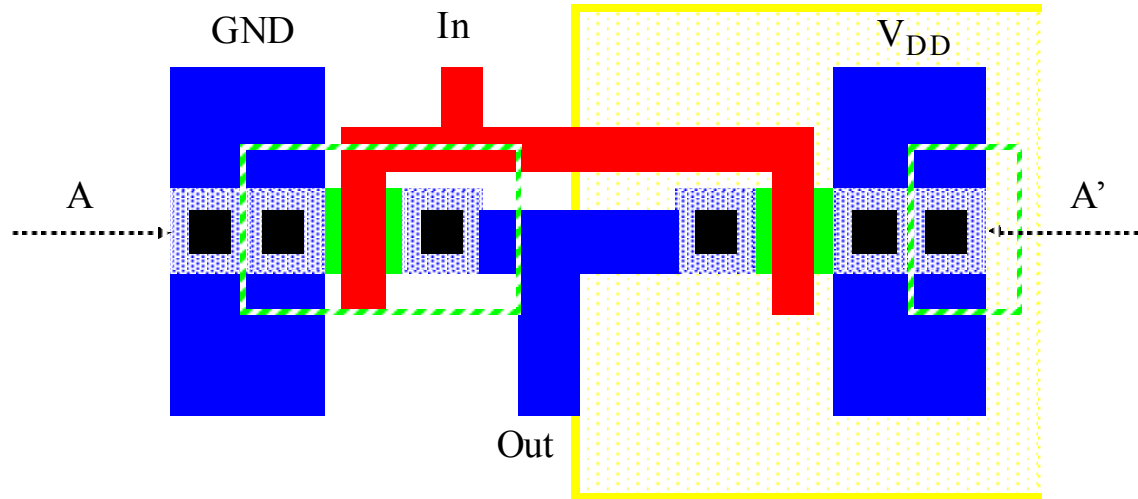


Select Layer

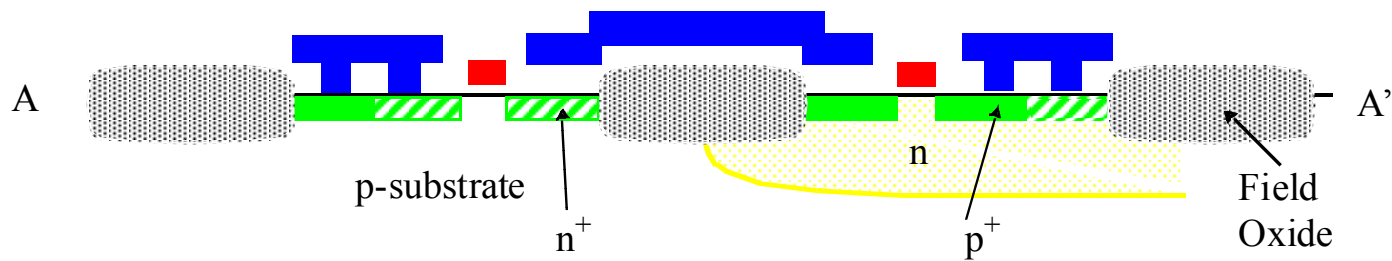




CMOS Inverter Layout



(a) Layout



(b) Cross-Section along A-A'





Content

- 1. 半導體元件簡介
- 2. 晶圓製作流程
- 3. Lithography概論
- 4. Etch概論
- 5. CVD / PVD 概論



課程材料及參考文件

* Major contents are revised from “Introduction to Semiconductor Manufacturing Technology” by Hong Xiao, Ph. D.

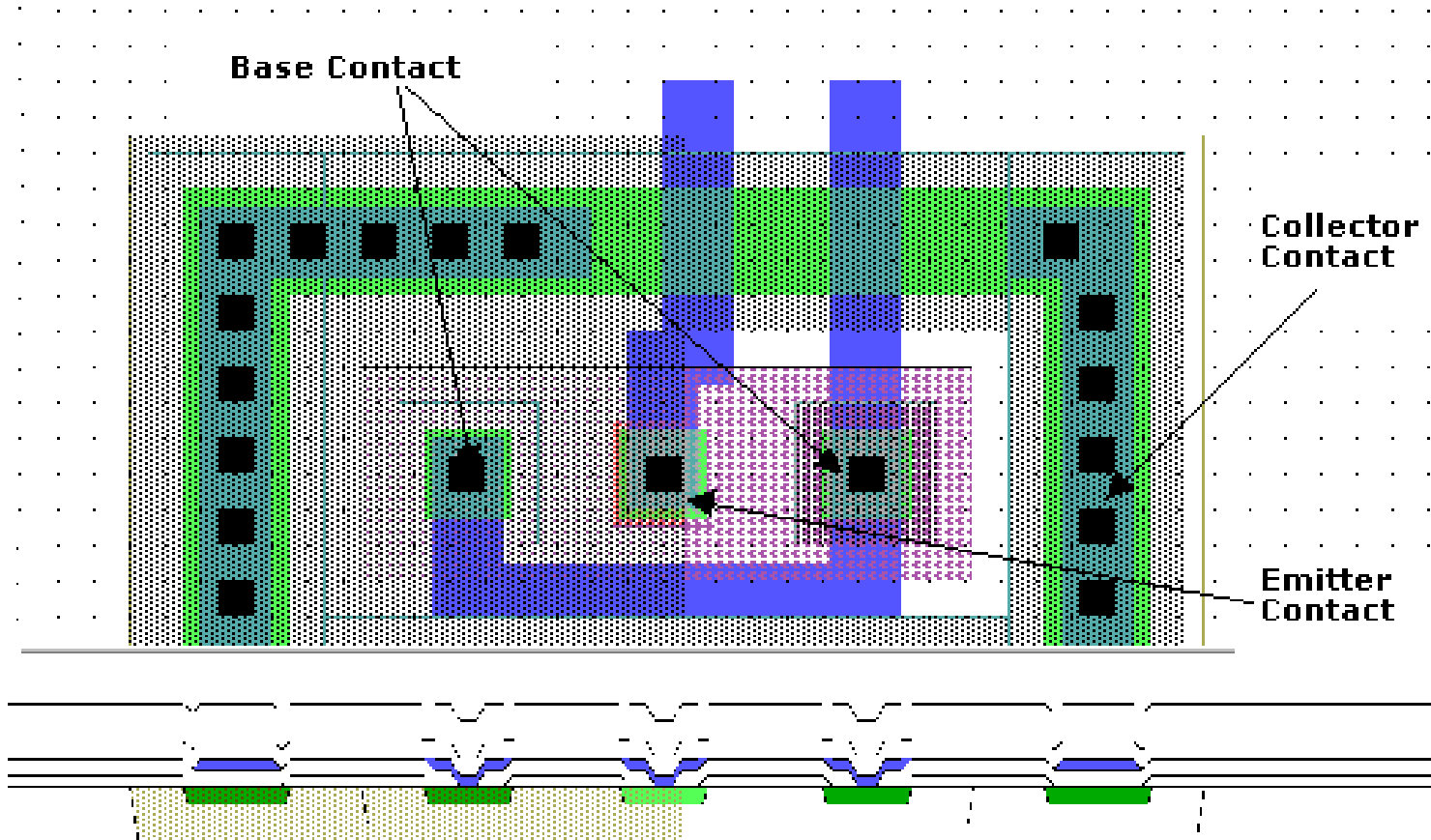
* STIP 科技產業資訊室 <http://cdnet.stpi.org.tw/>

* Silicon Technology and Manufacturing, Technology & Research at Intel
<http://www.intel.com/technology/silicon/index.htm>



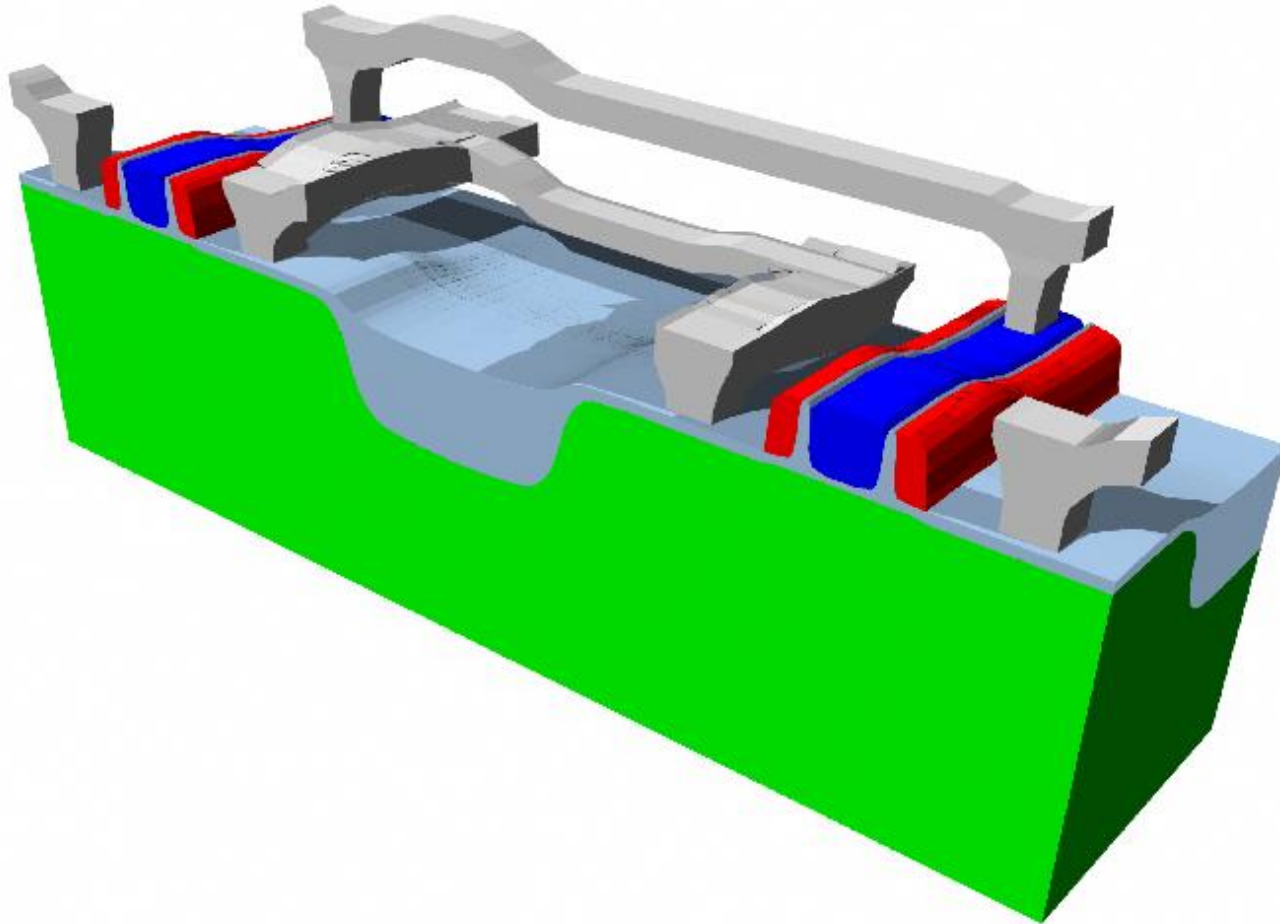


Bipolar Transistor Layout



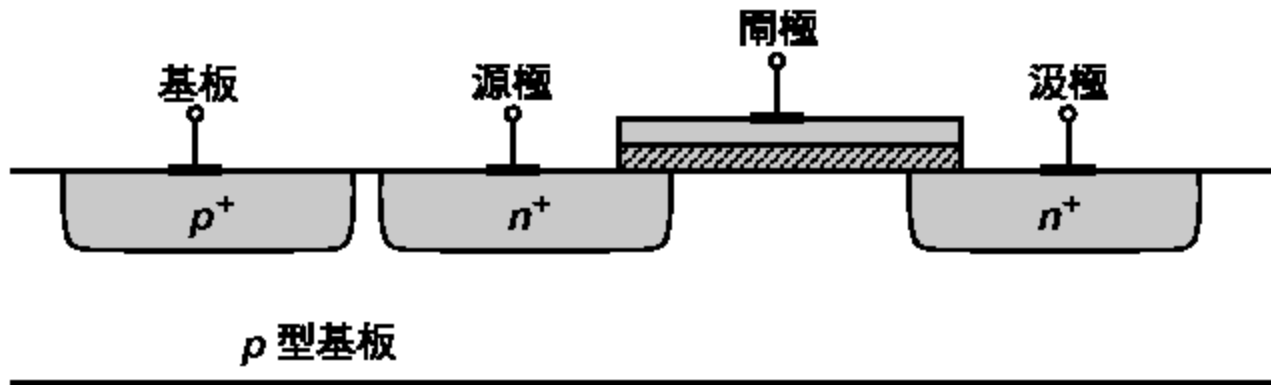


MOSFET結構





基板連接

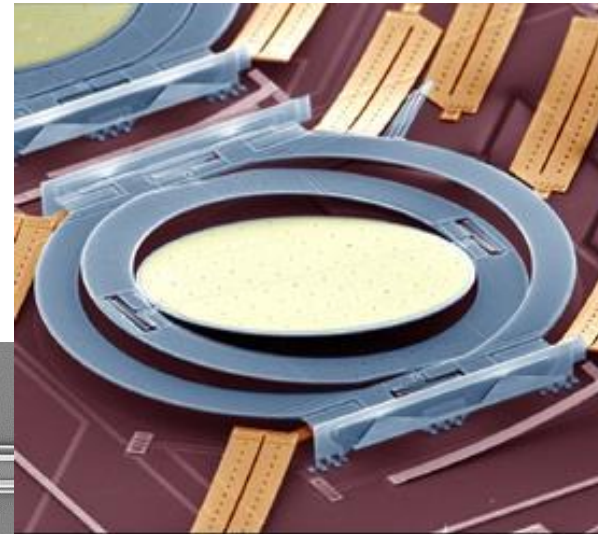
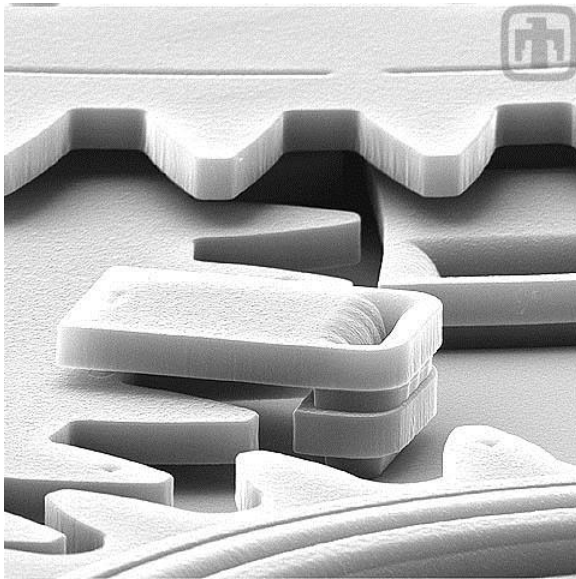


MOSFET為一個四端元件，一般NMOS電晶體基板連接至系統中最小的供應電壓，通常實際的連接是透過一電阻 p^+ 區域提供。





MOEMS Technology

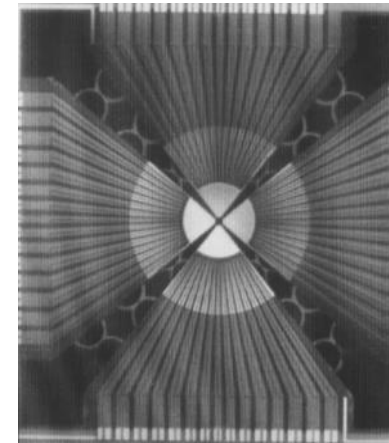
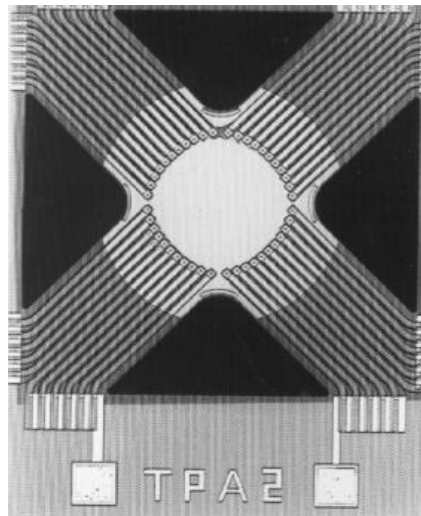
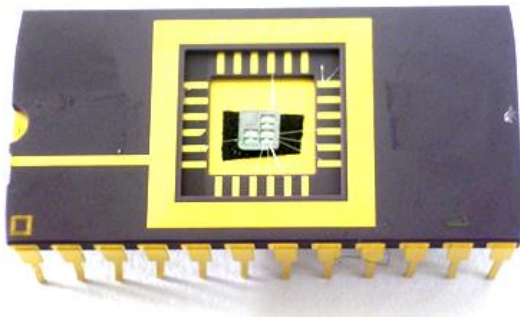
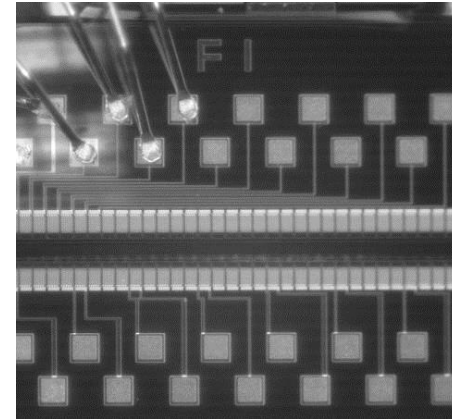
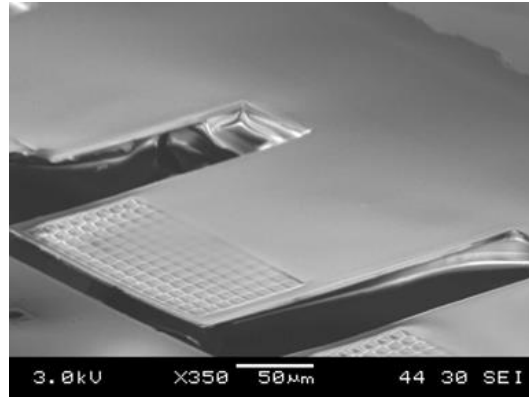
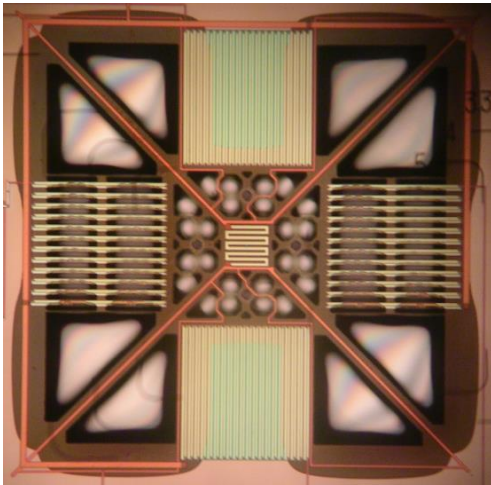


MEMS Overview



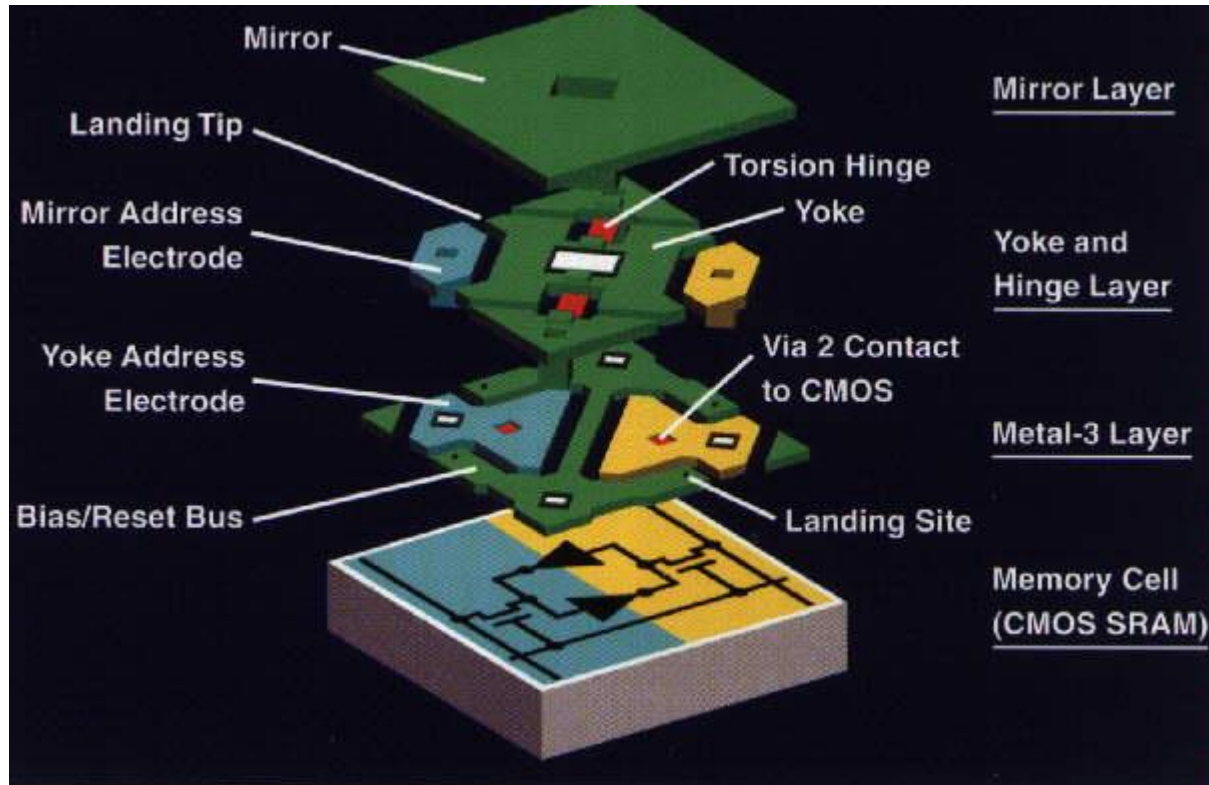


MEMS Sensors in NCUE





SOC of DMD

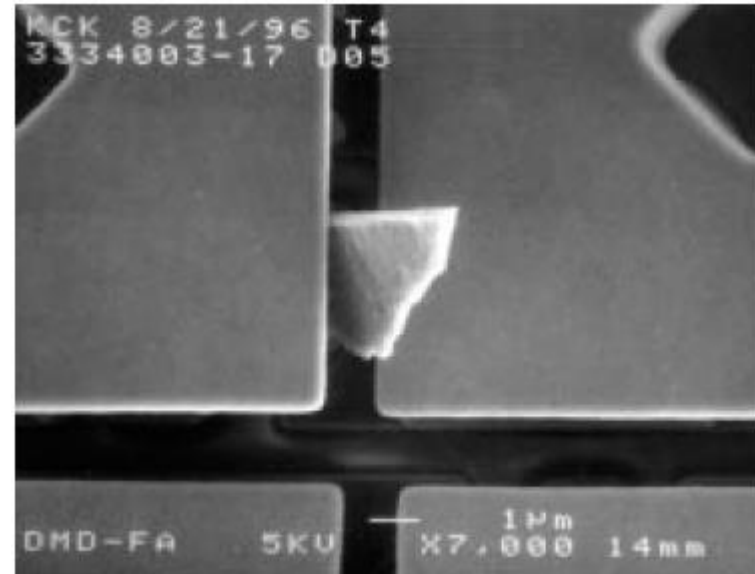
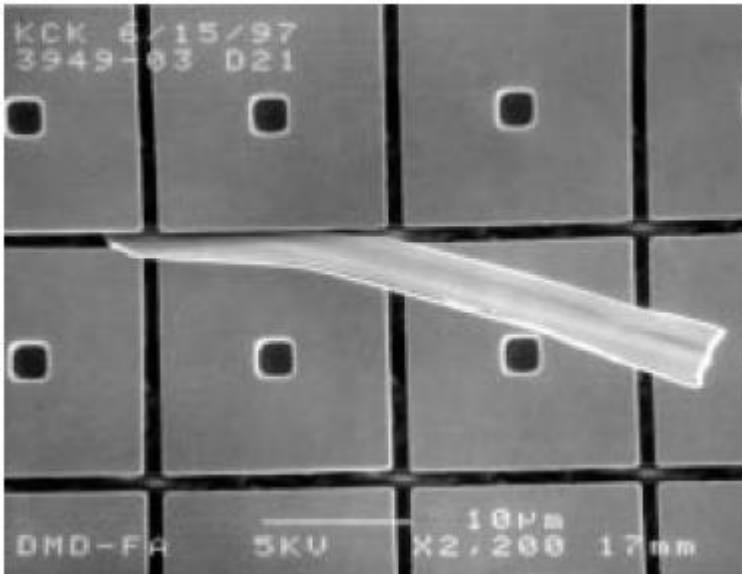


<http://www.dlp.com/>





DMD pixels with particle defects



MEMS Microphone

Under Development



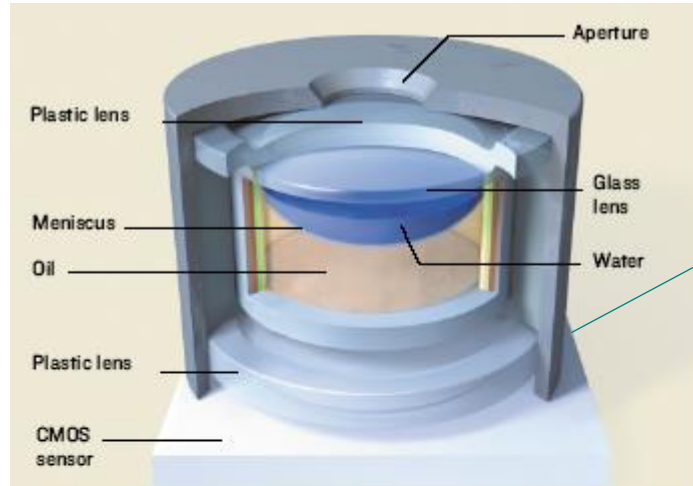
Figure 2. EmKay Sisonic Microphone, .This microphone is made from Silicon and is only millimeters large.

(Photo Courtesy of EmKay)



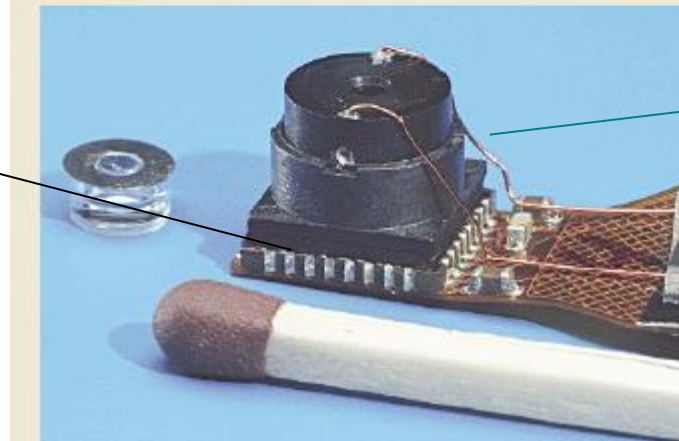


Fluidlenses 液體透鏡



MEMS

Driving Circuit



Optical Design

Temperature Compensation Analysis of Liquid Lens for Variable-Focus Control, Shu-Jung Chen and Chih-Hsiung Shen, Proc. SPIE Photonic West 2006. (EI)

光學模擬與公差分析於非球面廣角鏡頭之比較研究, 黃柏涵、沈志雄, 第二十二屆中國機械工程學會(2005)





What's the next ?

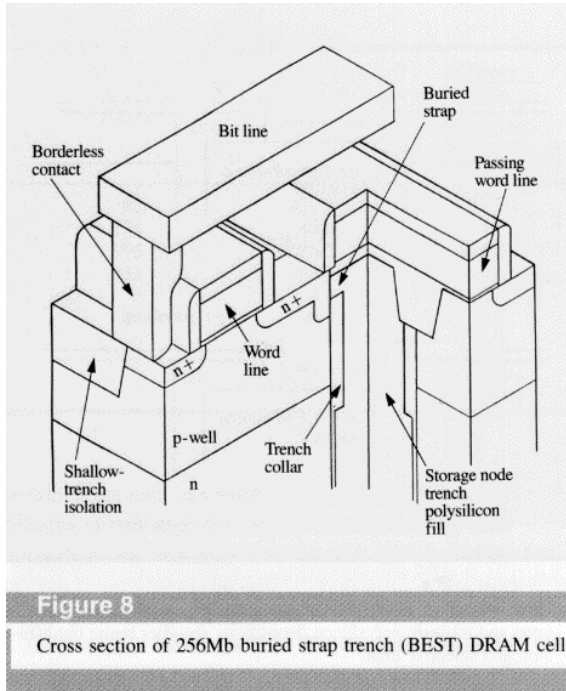


Figure 8

Cross section of 256Mb buried strap trench (BEST) DRAM cell.

IBM 256 Mb DRAM

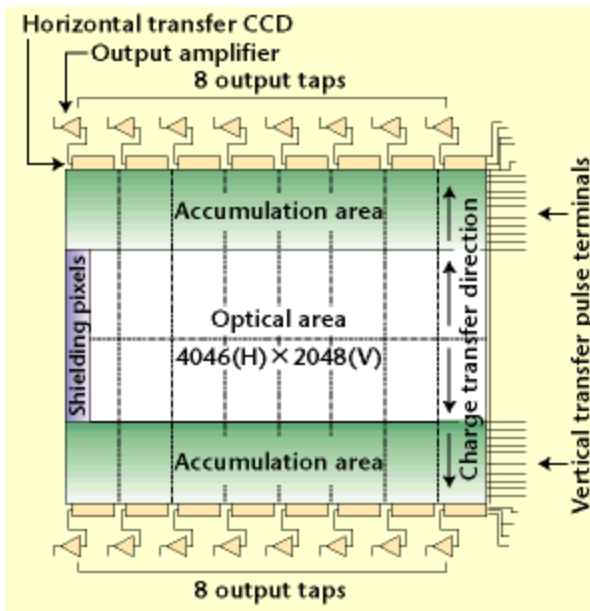
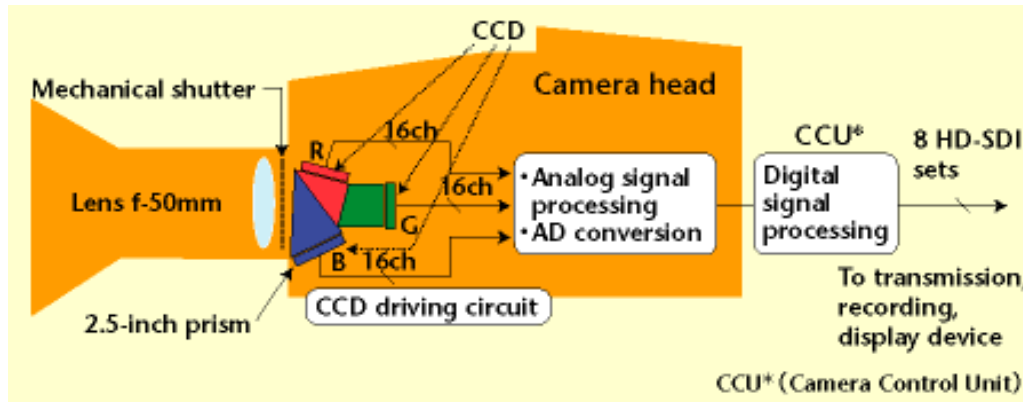


Nano CMOS



MOEMS

CCD

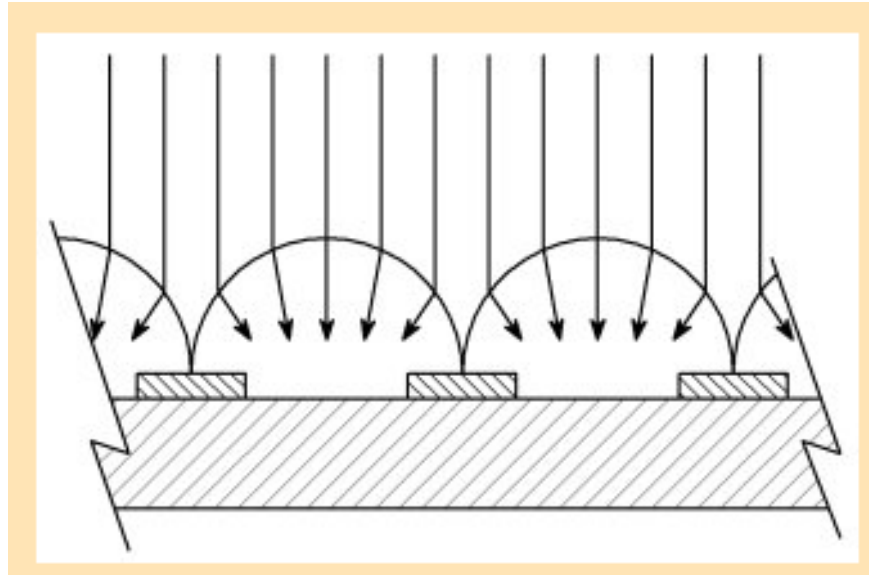


Total horizontal pixels	4,400 pixels/line
Total lines	2,250
Valid pixels	Approx. 8 million
Aspect ratio	16:9
Frame frequency	60 frames/second
Scanning system	Progressive scanning
Imaging system	RGB 3 CCDs





Microlenses



Microlens or Lenslet Arrays

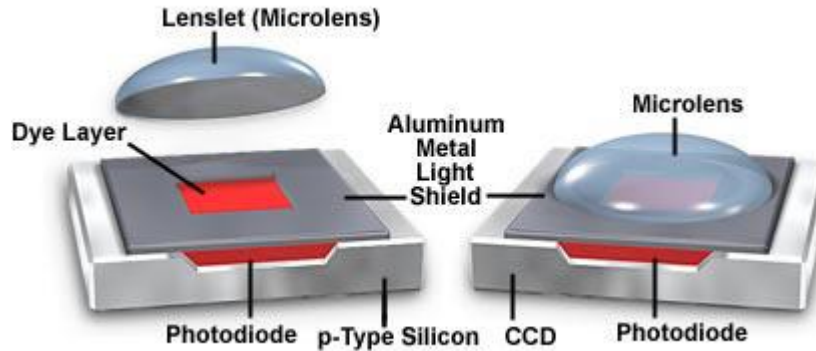
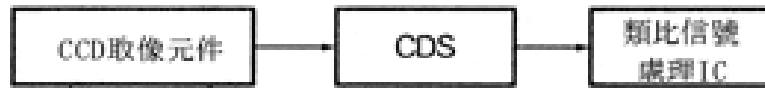


Figure 1

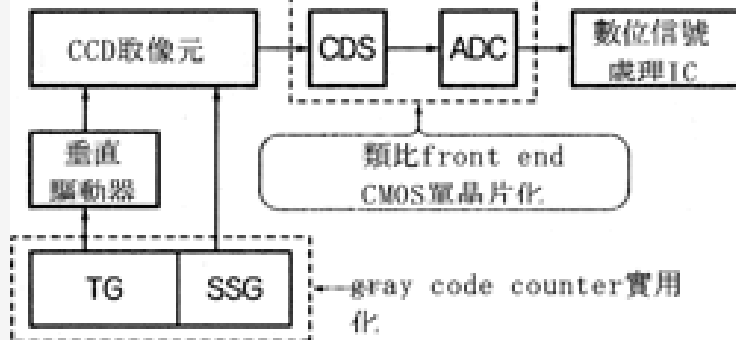


Circuit Structure

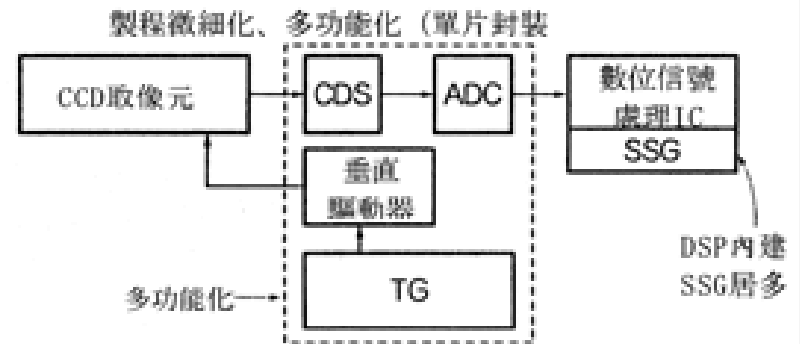


(a) 1980年代

內件水平驅動器、數位化、AFE的CMOS



(b) 1990年代



(c) 2000年代

CCD Structure

Anatomy of a Charge Coupled Device (CCD)

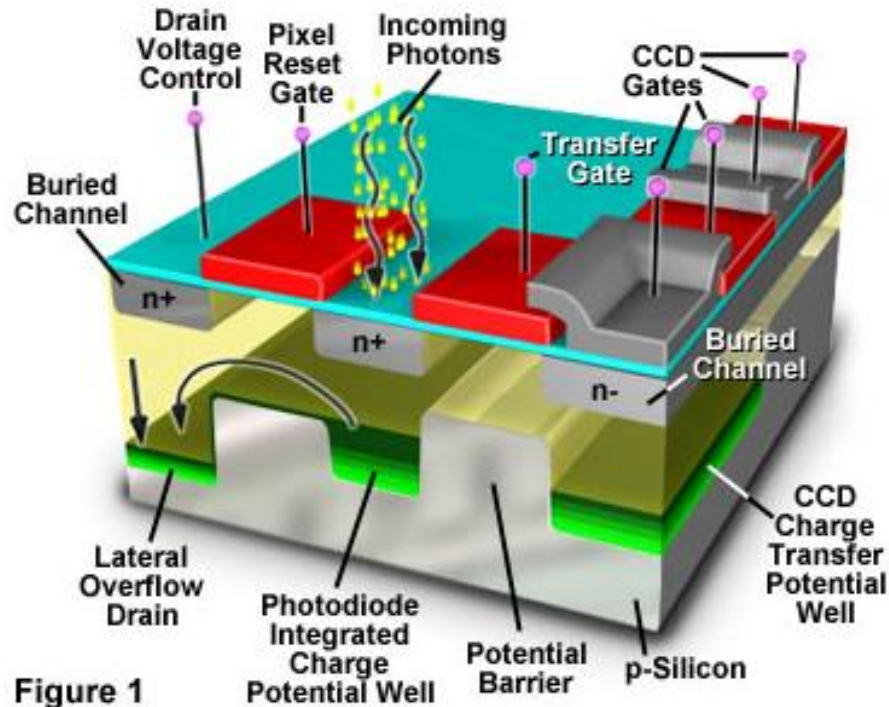


Figure 1

<http://micro.magnet.fsu.edu/primer/java/digitalimaging/ccd/virtual2/index.html>



Charge Couple Device

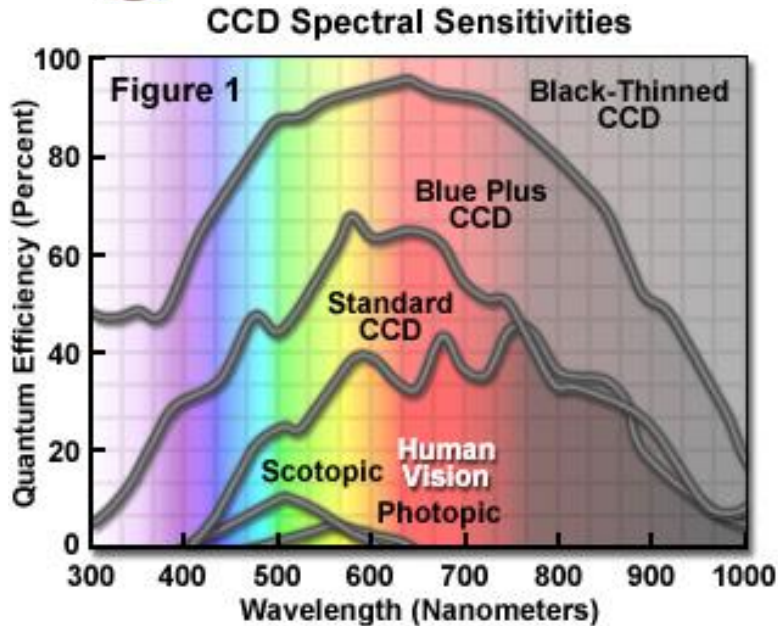


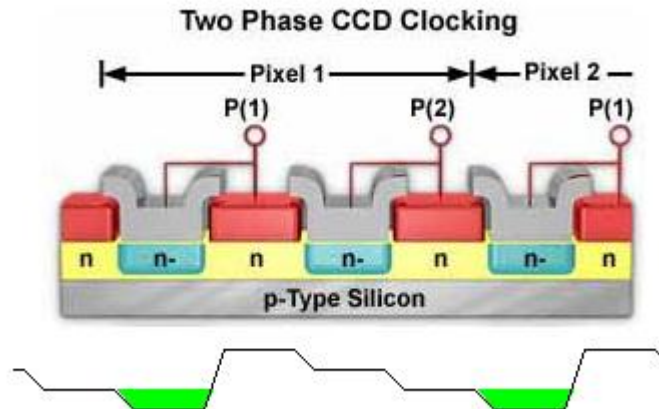
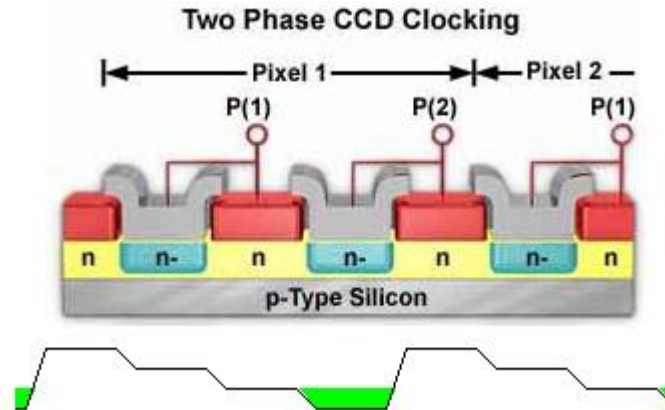
Figure 2

Recently, transparency of the channels has been increased with substantial improvement in blue-green sensitivity of some scientific-grade CCDs (Blue Plus curve in Figure 1) through the use of pioneering gate materials and proprietary phosphor coatings. Coatings of this type (Lumogen) are deposited directly onto the array surface and emit light in the 500 to 580 nanometer region when excited by short wavelength (120 to 450 nanometer) high-energy ultraviolet and visible light. Phosphors embedded within the coating produce a secondary fluorescence that is emitted in all directions, with only those photons entering the array being absorbed to yield a quantum efficiency of approximately 15 to 20 percent. The coatings are transparent to visible light, so they do not affect photon absorption at wavelengths exceeding 450 nanometers, producing an apparent spectral response range of almost 1000 nanometers (120 to 1100 nanometers).





CCD Clocking Schemes

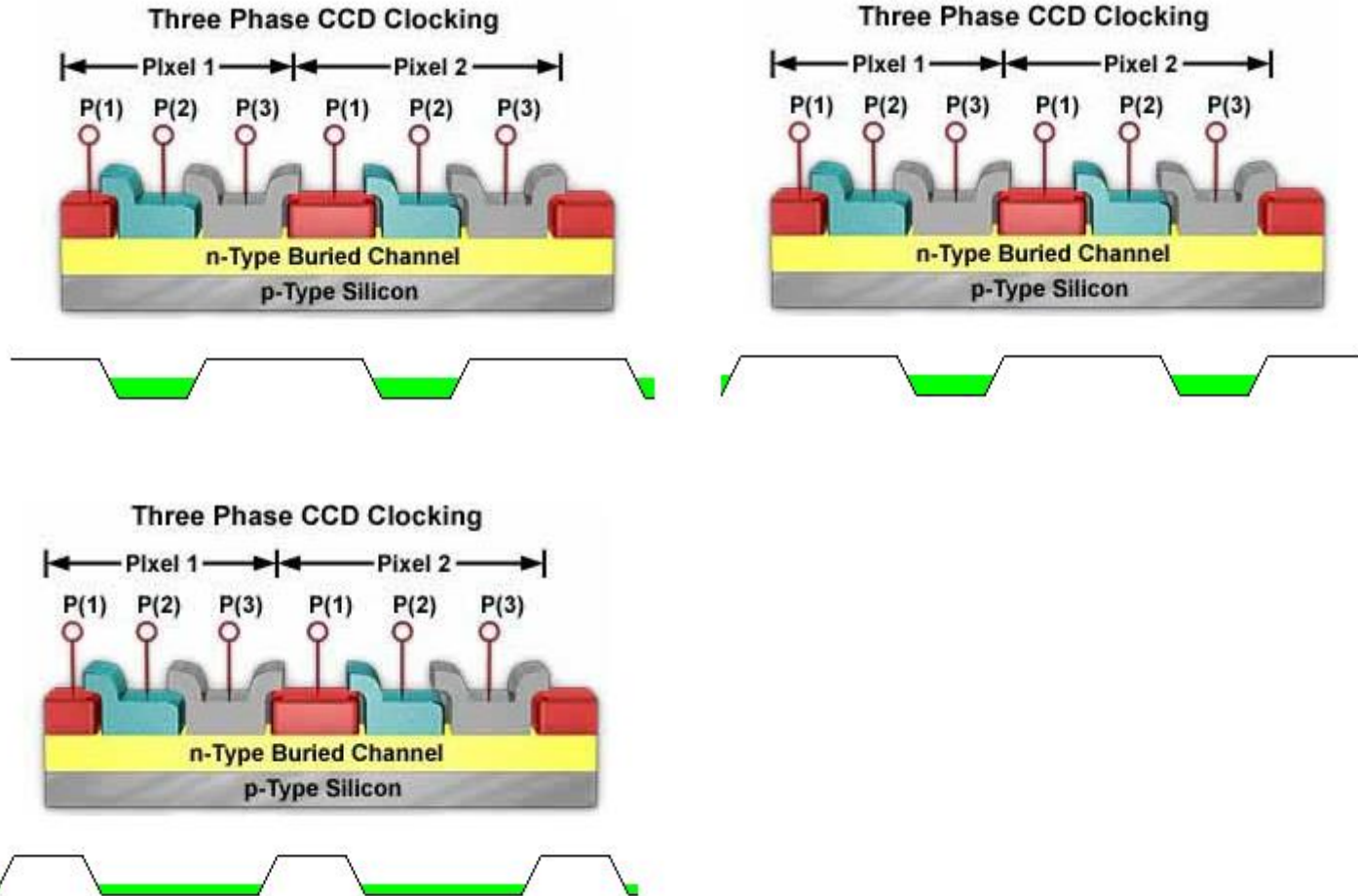


<http://micro.magnet.fsu.edu/primer/java/digitalimaging/ccd/shiftregister/index.html>



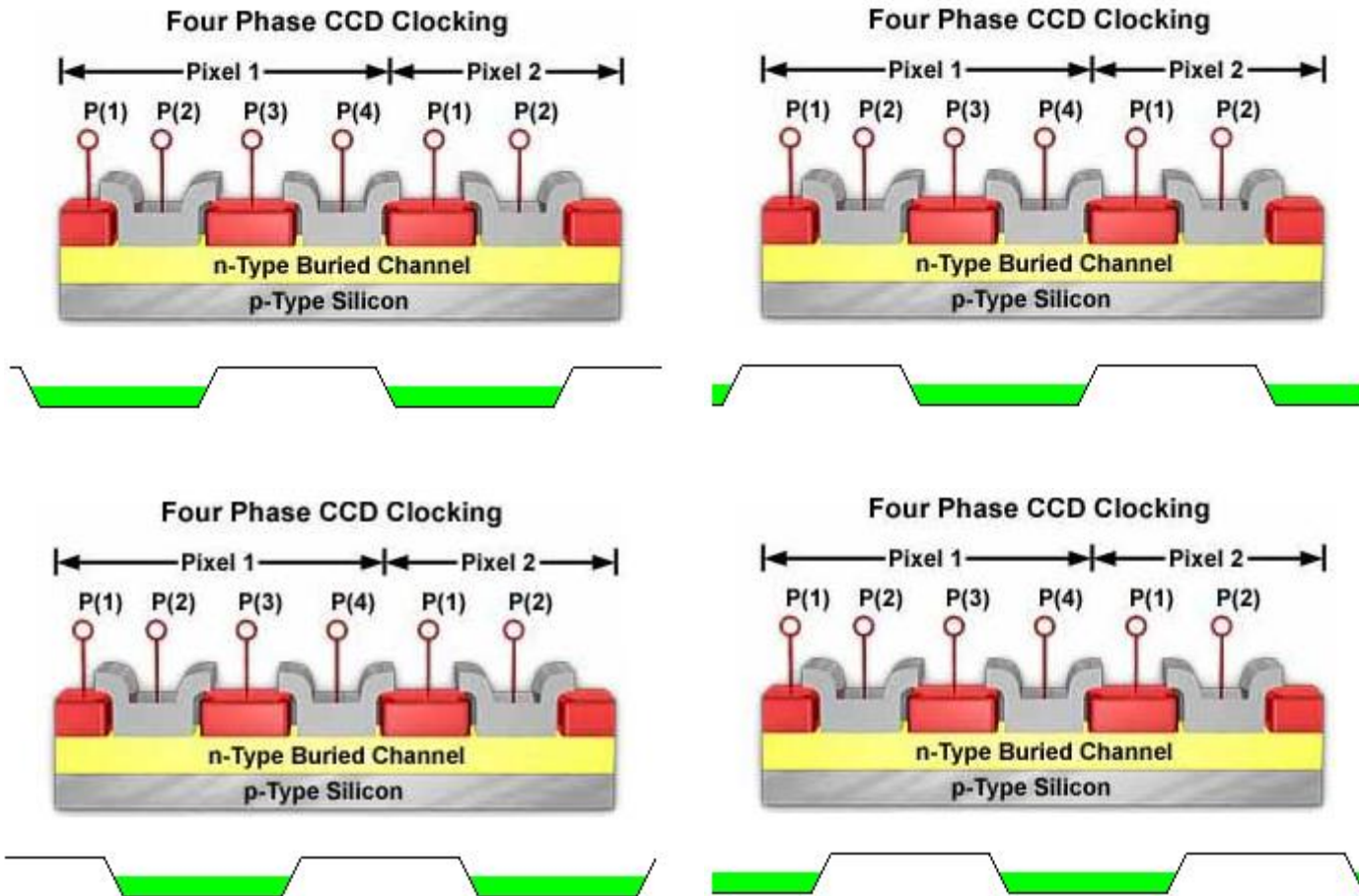


Three Phase CCD Clcking



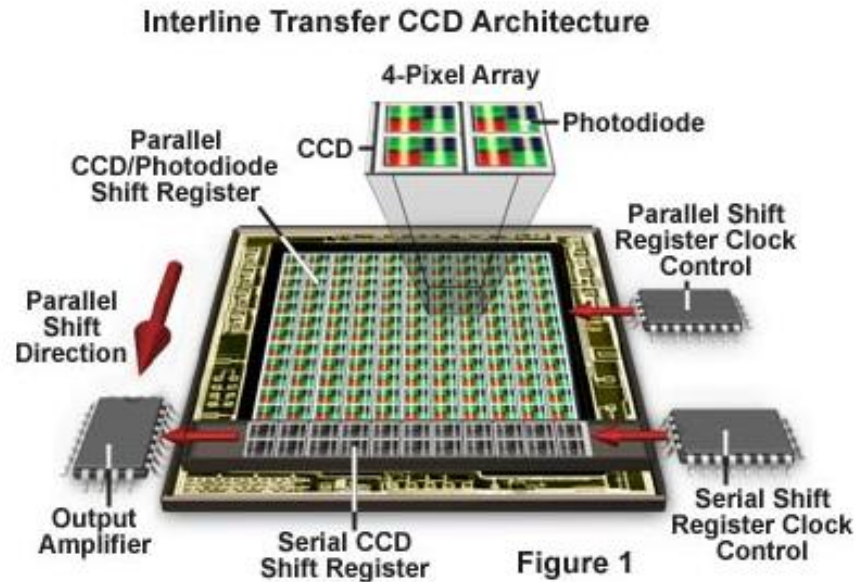


Four Phase CCD Clocking





Interline Transfer CCD Architecture



Masked regions of the pixels are positioned alongside the photodiode elements in an alternating parallel array traversing the length of the CCD's vertical axis. Photodiodes in the array comprise the image plane and collect incoming photons projected onto the CCD surface by the camera or microscope lenses. After image data has been collected and converted into electrical potential by the image array, the data is then quickly shifted in a parallel transfer to the adjacent CCD storage area of each pixel element. The storage portion of the pixel element is illustrated as a cluster of gray-scale elements covered with an opaque mask adjacent to the red, green, and blue photodiode elements in each CCD. These pixel elements combine to form vertical columns that run from the serial shift



Frame Transfer

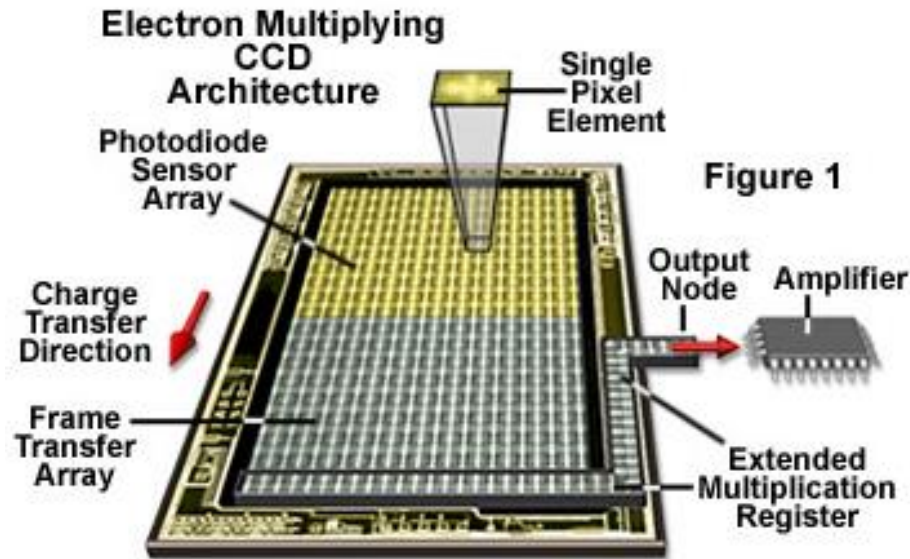


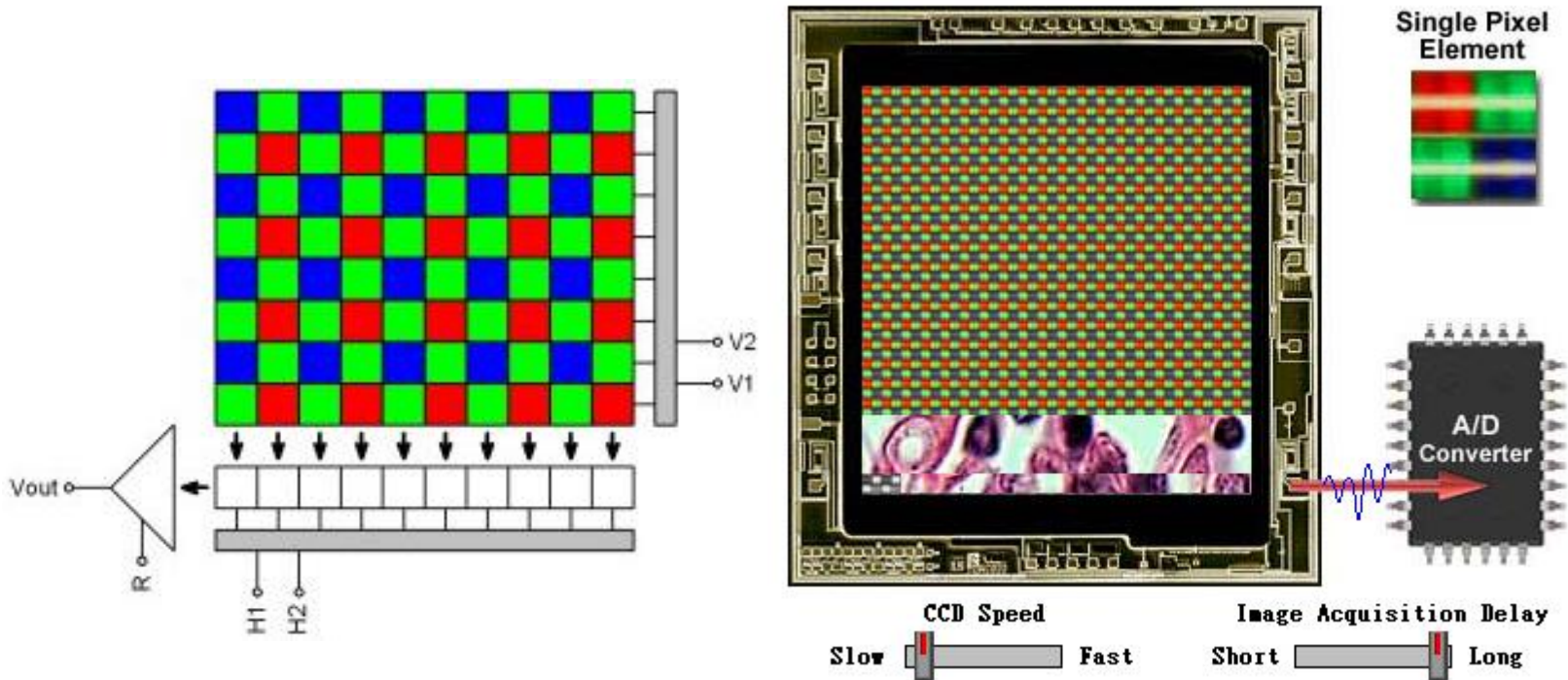
Figure 1

The **image array** consists of a light-sensitive photodiode register, which acts as the image plane and collects incoming photons projected onto the CCD surface by the camera or microscope lenses. After image data has been collected and converted into electrical potential by the image array, the data is then quickly shifted in a parallel transfer to the **storage array** for readout by the serial shift register. Transfer time from the image-integrating array to the shielded storage array is dependent upon the pixel array sizes, but is typically on the order of 500 microseconds or less. The storage array is not light sensitive in most frame-transfer CCD designs, however some arrays are not equipped with an integral light shield. Arrays of the this design are capable of being operated in either full-frame or frame-transfer modes.





Full-Frame CCD Operation



The pixel array illustrated in the full-frame CCD above consists of a parallel shift register, onto which images are optically projected by means of a camera lens or microscope optical train. In this configuration, all of the photodiodes in the pixel array collectively act as the image plane and are available for detecting photons during the exposure period.





Saturation and blooming

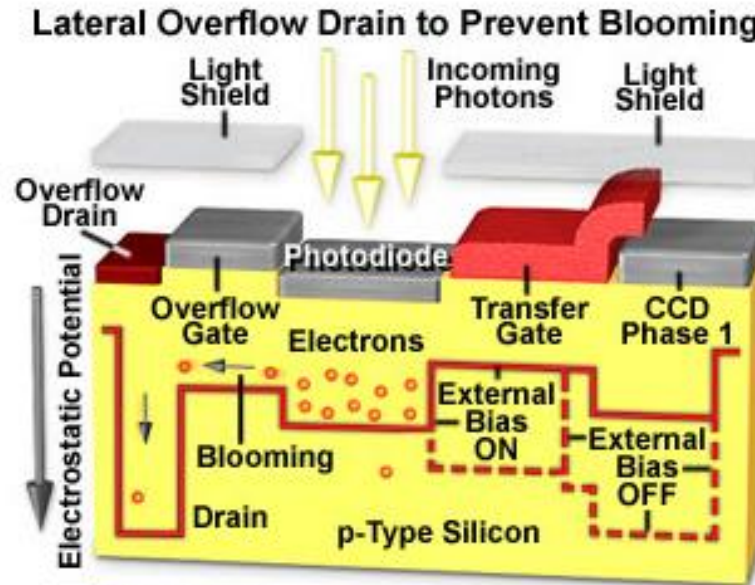


Figure 3

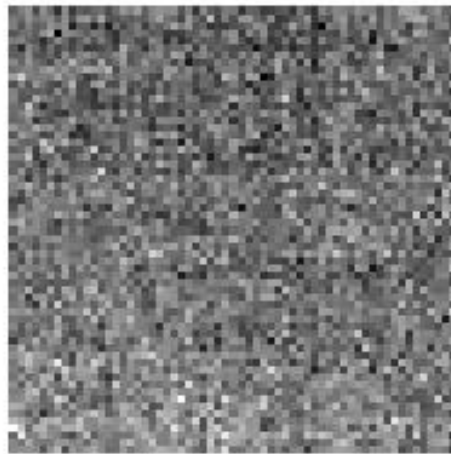
Saturation and blooming are related phenomena that occur in all charge-coupled device (CCD) image sensors under conditions in which either the finite charge capacity of individual photodiodes, or the maximum charge transfer capacity of the CCD, is reached. Once saturation occurs at a charge collection site, accumulation of additional photo-generated charge results in overflow, or blooming, of the excess electrons into adjacent device structures. A number of potentially undesirable effects of blooming may be reflected in the sensor output, ranging from white image streaks and erroneous pixel signal values (as illustrated in Figure 1) to complete breakdown at the output amplification stage, producing a dark image.



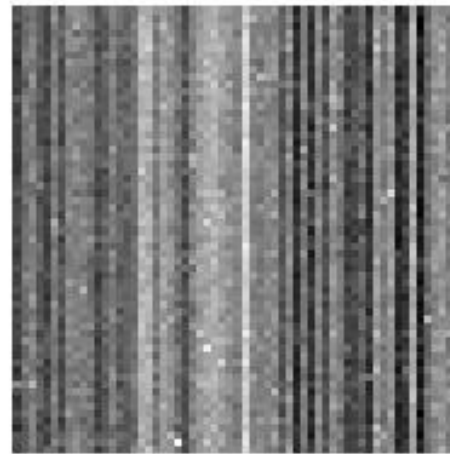


Fixed Pattern Noise

- Fixed variation in offset and gain from pixel to pixel
- Can be caused by many physical differences in the sensors and circuitry.



CCD FPN



CMOS FPN



Canon Eos D30 測試報告 - 前導篇

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※Canon EOS D30主要的特長

- 採用新開發的大型CMOS sensor
- 同級品中世界最小、最輕量的高剛性機身
- 繼承了EOS的基本操作
- 高速、高性能的3點測距AF
- 豐富的攝影模式
- 35分割的評價測光
- E-TTL自動調光系統
- 採用最適合大量攝影的compact flash card
- 符合業界標準規格
- 對應USB
- 應用軟體的充實





CMOS Imager

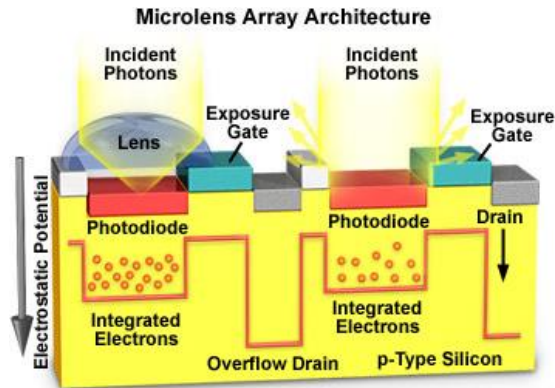


Figure 2

Microlens Array on Photodiodes

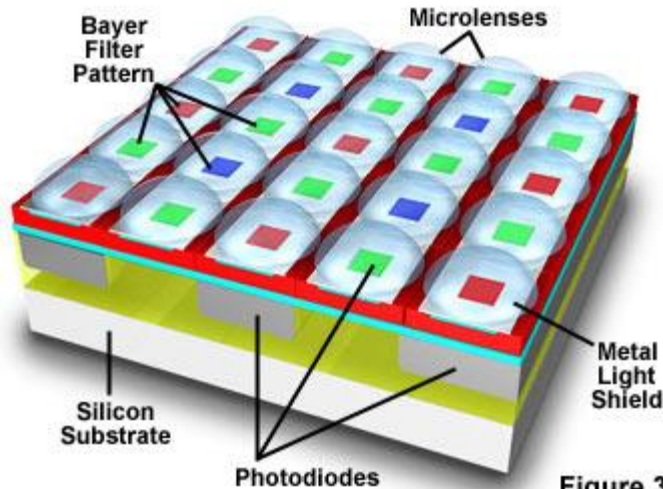


Figure 3

CMOS Image Sensor Integrated Circuit Architecture

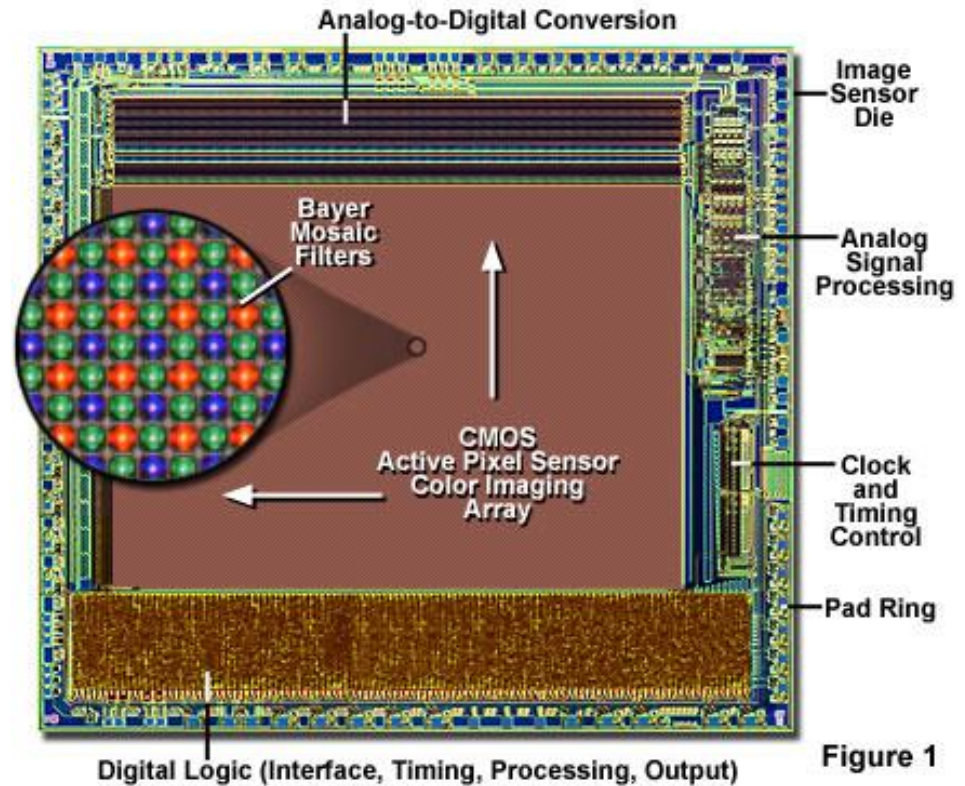


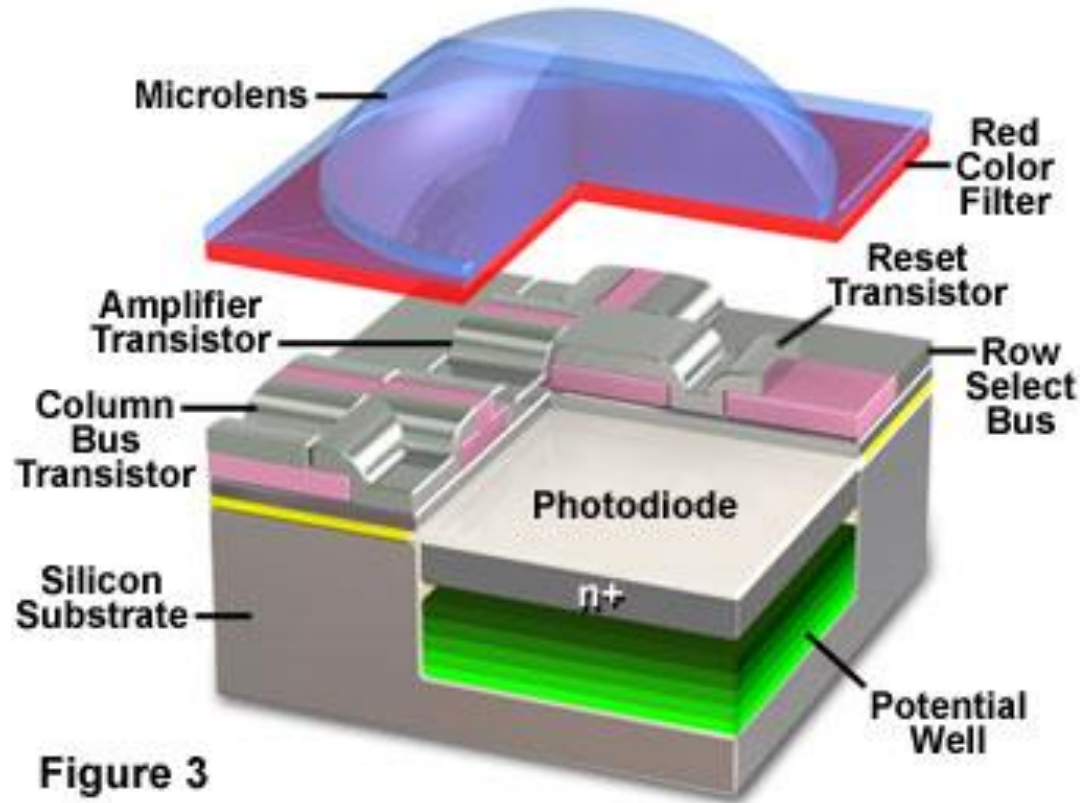
Figure 1





Structure of CMOS Imager

Anatomy of the Active Pixel Sensor Photodiode





CMOS Imager IC Block

